ONE MEGACYCLE UNIVERSAL LOGIC MODULES

A thesis submitted
In partial fulfilment of the requirements
for the Degree of
MASTER OF TECHNOLOGY IN ELECTRICAL ENGINEERING

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by

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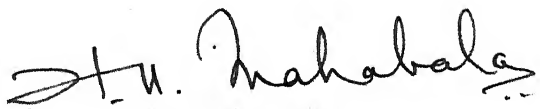
CERTIFICATE

Certified that this work on "One Megacycle Universal Logic Modules" has been carried out under my supervision and that this has not been submitted elsewhere for a degree.



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LIST OF SYMBOLS

V_{cbo} = Measured breakdown voltage collector to base emitter open.

V_{ceo} = Measured breakdown voltage collector to emitter base open.

V_{cc} = Collector supply voltage.

V_{ces} = Collector to emitter saturation voltage.

V_{bes} = Base to emitter saturation voltage.

V_{ob} = Reverse base bias voltage.

V_{TF} = Forward voltage at threshold of conduction.

V_{bb} = Base supply voltage.

V_{TR} = Reverse threshold voltage.

I_c = Collector current (D.C.)

I_{cl} = Collector leakage current.

I_{ces} = Collector current for saturation.

I_{bl} = Base leakage current.

I_k = Input current.

I_{LO} = Load current in '0' state.

I_{L1} = Load current in '1' state.

V_0 = Output voltage for a '0' state.

V_1 = Output voltage for a '1' state.

I_s = Current from the base bias source.

n_P = Power supply tolerance.

n_R = Resistor tolerance.

N_R = Resistance tolerance modifier.

n_C = Capacitor tolerance.

N_C = Capacitance tolerance modifier.

N_P = Power supply tolerance modifier.

R_K = Coupling resistor.

R_C = External collector resistor.

R_B = External base resistor.

R_L = Load resistor.

t_r = Rise time.

t_s = Storage time.

t_f = Fall time.

T_D = Pulse duration.

T_R = Recovery time.

β = I_c/I_b = Common emitter current gain in transition region.

β_F = I_c/I_b = Current gain in saturation region.

γ = Ratio of current through collector resistor for a '0' to that for a '1'.

* Above a symbol indicates maximum value.

$_-$ Below a symbol indicates minimum value.

Numerical subscript to a subscript indicates the transistor to which it pertains.

Numerical quantities '0' and '1' along a subscript indicate that they belong to '0' or '1' state.

SYNOPSIS

ONE MEGACYCLE UNIVERSAL LOGIC MODULES

Lieutenant Subhendu Majumdar

The need for a logically complete set of logic circuit modules for building digital systems is well established. This thesis concerns with the design and fabrication of such a set using indigenous components.

The TRL family used provides good fan-in (four) and fan-out (four) capabilities. Silicon p-n-p transistor type 2N995 (indigenously available) provides an operating temperature range of 0° C - 65° C. Negative logic is employed (with '0' corresponding to zero volts and '1' to -3 volts (-3 to -6V)).

Design by absolute worst case analysis technique is used allowing for $\pm 5\%$ variation in power supply voltages and component values. Noise immunity of 1V step has been achieved.

Set includes NOR, flip flop, one-shot, inverters and lamp driver circuits and are fabricated by printed circuit technique.

Detailed test procedures for each module and results thereof are reported.

CHAPTER 1

INTRODUCTION

Ditigal techniques are finding increasing use in a wide variety of engineering applications particularly in the solution of timing and control problems. Digital systems are used to control automatic processes in mass production techniques, control and regulate complex processes in oil refineries and other chemical industries, and have a host of other industrial applications. Another very important use of digital circuits is in data processing and information handling operations in weapon control, prediction and space communication systems. In fact the birth of the digital computer in its present form has been from the computational requirements of military problems. Extensive use of digital computers necessitates diverse use of digital circuits.

The present day computer is not designed as one big circuit, but as interconnection of small units each capable of performing a small special function otherwise referred to as modular design. It is proposed to develop such small units called basic modules each of which is capable of performing a special function. Once the whole range of basic modules are developed to perform any logical function, it should be easy to build up a small educational digital computer.

These modules can be used in a wide variety of applications and the designer is not always in a position to know the ultimate specific use of the modules. For example, they can be used in

communication systems or in sample data control systems or in similar applications. The universal utility of basic modules places three important requirements for the basic modules to be developed.

(i) Logical completeness:- The set should be logically complete so that any digital function can be achieved by interconnecting these modules.

(ii) Performance specifications:- These must be accurately specified so that the user can expect the system he has to design to work satisfactorily.

(iii) Reliability:- The module must perform its function reliably over the entire range of specifications such as under worst conditions of component value deviations from its normal figure, environmental conditions and loading.

With these requirements in view the basic modules to be developed at the Indian Institute of Technology, Kanpur are to be a set of packaged digital circuits for building general digital systems. They have to be designed with the worst case design philosophy giving due allowance to component variation, extreme changes of environmental conditions, power supply variations and system noise.

With the advent of integrated circuits in more advanced countries basic I.C. modules for performing special logical functions are economically available and basic modules with discrete components are only used for class-room

demonstration purposes. In India, however, there is no facility of manufacturing integrated circuits and with the present state of the art there seems no possibility of large scale development of integrated circuits in the near future. Under these conditions, development of the digital systems industry to a mature state, requires, the development of basic modules with discrete components; hence an attempt is made to develop a set of basic modules using indigenously manufactured discrete components.

Since integrated circuits will eventually be manufactured in India, the ideal situation would be to have these basic modules compatible with the integrated circuits so that a switch over at a later date will be easy.

The basic modules are to be fabricated by using printed circuit technique. Interconnection between cards is to be done with connectors and all the component materials should be indigenously available. The mechanical rigidity, packaging density, maintainability and overall cost should be considered in design. Sufficient test points should be provided to aid trouble shooting.

Speed is a very important criterion in the selection of the transistors to be used and this in turn decides the logic family to be used. Selection of logic family has been dealt in detail by Mr. C.V. Singh in the logical design of a small educational computer. Here again, cost, reliability and availability of components from indigenous sources have

to be taken into consideration.

These basic modules have to be tested under extreme changes of environmental conditions with pessimistic limits of component values and power supply variations.

For good reliability component specifications have to be derated by 20% of actual test figures. Detailed test procedures for testing (exhaustive or sample) have to be given.

CHAPTER 2

SELECTION OF LOGIC FAMILY AND TRANSISTOR

The main function of a logic system is to arrive at a logical decision as a combination of conjunction (AND) disjunction (OR) and negation (NOT). In present day computers all logical functions are performed by repeated use of one basic logic circuit, namely, NOR or NAND.

At present the various logic families known are

(1) Diode transistor logic DTL

(2) Direct coupled transistor logic DCTL

(3) Transistor transistor logic TTL also known as Transistor Resistor Logic TRL

(4) Emitter coupled logic ECL

(5) Resistor transistor logic RTL

(6) Current mode logic CML

An exhaustive comparison between the families is difficult because while comparing one family to another one must take into account the following

(1) Speed (propagation delay)

(2) Noise immunity

(3) Fan-in and fan-out

(4) Power supply requirements

(5) Power supply when packaged

(6) Suitability for integrated fabrication

(7) Reliability

(8) Cost

Choice of a family is also dependent on availability of suitable transistors and hence an examination of transistor types available indigenously will now be presented.

The important parameters of switching transistors of indigenous manufacture are given in Appendix 1 and their suitability regarding each parameter will now be discussed.

Since the logic levels chosen are (0 to -.3V) corresponding to logical 0, -3V (-3 to -6V) for logical 1, the chosen power supply being -6V, all transistors are suitable from the point of view of breakdown voltages.

A rough estimate indicates that the maximum current to be carried by any transistor will not exceed 12 mA as discussed in detail in Chapter 5. All transistors can handle this current.

A low V_{ces} ensures a low zero level and decreases the possibility of transistor in saturation turning on a subsequent stage. This parameter classifies the listed transistors into the following categories:

	2N404	2N428	2N995	CIL511	CIL701	CIL711
V_{ces} at	-.1V	-.35V	-.2	.25	.4	.4
I_c in mA	12	200	20	25	25	30
I_b in mA	.4	10	2	2.5	2.5	1.5
Remarks	good	average	fair	fair	average	average

This requirement restricts the choice of transistors to 2N404, CIL511 and 2N995.

A low propagation delay permits the use of higher operable frequencies and a rough estimate is that the propagation delay

per stage should not exceed 1/3rd the duration of one time period. This requirement classifies the transistor into the following categories:

	2N404	2N428	2N995	CIL511	CIL701	CIL711
Stage delay	28μs	100μs	440 ns	2240 ns	400 ns	400 ns
Remarks	poor	poor	good	average	good	good

This requirement restircts the choice of transistors to the following types 2N995, CIL511, CIL701, CIL711. Here it is worthwhile to mention that though the stage delay of CIL701 and CIL711 is listed in the 400 ns, actual measurement on a random batch of 10 did show a lot of discrepancies from specifications. The results of the measurements have been tabulated in Appendix 2 and lead to the conclusion that CIL511 though not listed as a switching transistor is just as good as CIL701 or CIL711 for system voltages in use. The comparative performances are listed below.

	CIL511		CIL701		CIL711		2N995	
	Min	Max	Min	Max	Min	Max	Min	Max
Stage delay in ns in a batch of 10	2.4	4.0	3.33	5.3	3.32	4.9	.30	.45
Remarks	Fair		average		average		good	

Therefore, speed requirement places 2N995 as by far the best available transistor in the local market. Its selection, however, involves one major sacrifice.

It was pointed out before that basic modules when developed should be compatible with integrated circuits. Since

the integrated circuits that will most probably be manufactured in India are of the n-p-n type, selection of 2N995- a p-n-p transistor- will make the basic modules incompatible with the integrated circuits Immediate use for the basic modules require high speed and as such this incompatibility has been tolerated. Further, 2N995 is a silicon device which brings in associated advantages in increased range of operating temperatures.

And now comes the most important criterion in selection and that is cost. A comparative cost figure is listed below:

2N995	CIL511	CIL701	CIL711
Rs 7.50	Rs 5.50	Rs 12.30	Rs 19.50
Fair	good	poor	poor.

From the point of view of economics, the two most likely choices are 2N995 and CIL511. However, the increase in cost in the selection of 2N995 is offset by the increase in speed.

Since the project should do the best under Indian conditions, perhaps, delivery time should also be a criterion in the choice of transistors and components. Transistor finally chosen was 2N995 p-n-p silicon planar epitaxial transistor.

A designer of computer logic circuitry continually tries to handle more bits of information per unit cost per unit time. The emphasis in a particular system will be on either or both of the above requirements. Component count in a circuit, component reliability, ease of manufacture, power dissipation and maximum fan-in and/or fan-out are other factors affecting the choice of a family.

When speed fan-in and fan-out are not of prime importance RTL circuitry is commonly used because of its simplicity, low cost and reliability. The speed of RTL logic circuits is device dependent upto the point where time constants of load resistors and capacitors limit the speed. Faster transistors give faster RTL circuits. Use of speed up capacitors increases the speed significantly but the associated problem of cross talk and noise far outweigh the gain in speed. As development of 1 Mc/s logic blocks is being attempted the available transistor does not permit the use of RTL logic family.

Non-availability of fast computer diodes of indigenous manufacture excludes the possibility of selection of a logic family using diodes. This rejects the selection of DTL family though their use permits a gain in speed and fan-in and fan-out capabilities.

The speed of logic circuits in general depends a great deal on external circuitry and low output impedance is important. The high speed operation involves lower load resistance, lower load capacitance and higher currents and the associated penalty is increased power dissipation. Substantial increase in speed can be achieved by using CML or emitter coupled transistor logic but the difficulties in this configuration are that the V(0) and V(1) levels in the output differ from those of the input. Therefore, avalanche diodes and emitter followers must be used to provide input output compatibility. The possible higher speed obtainable with ECTL logic family is offset by the increased power dissipation and increased component count.

The main difference between the TRL logic family and RTL logic family is that in the former there is one transistor for each input whereas in RTL logic family the number of inputs in a gate is equal to the fan-in of the gate. This increases the cost of the system but but the advantage gained is increased speed. Though the RTL is a much cheaper form of logic family, its limitations are lower speed and it requires a higher minimal β transistor. The configuration is similar to DCTL circuits but the problems of base current hogging in DCTL circuits is circumvented by the use of base padding resistors. Another distinct disadvantage of DCTL circuits is that the two discrete levels of DCTL circuits are V_{ces}. and V_{bes}. In order to have an appreciable noise margin, this difference should be as large as possible. This makes the circuit more susceptible to noise. An appreciably high value of base padding resistor in TRL circuits permits the 1 level to differ appreciably from V_{bes}. The family chosen is the TRL family and the V(1) level is permitted to be in between -3 volts to -6 volts (V_{cc}).

In TRL family each transistor can at most have one input. The fan-in of a gate is increased by increasing the number of transistors. It has been shown by Mr. C.V. Singh in his M.Tech. thesis that with a minimum β of 35 the max. fan-in for TRL circuits is limited to 4. Under the conditions the maximum fan-in permissible for TRL circuits is 4. The maximum fan-out permissible depends on the range of V(1) level. In the present system, with the V(1) being in the range -3V to -6V, the fan-out is limited to 4 gates.

As diodes are not being used to clamp the output level in the present system, the output level will vary from V_{cc} (-6V) for no load to -3V for maximum fan-out.

Another important factor influencing the choice of TRL family for basic modules is the ease with which other basic digital circuits can be constructed by interconnecting TRL family. This advantage really pays full dividends in integrated circuit manufacture where an extra transistor is, perhaps, just as cheap as an extra resistor.

CHAPTER 3

SPECIFICATIONS

The basic modules to be constructed consist of the following blocks:

S.No.	Description	Function	Logic Symbol
1	TRL gate	logical element	Fig. 3.1
2	Inverter	inversion element	Fig. 3.2
3	Flip Flop	storage element	Fig. 3.3
4	One shot	delay element	Fig. 3.4
5	Lamp driver	indication element	Fig. 3.5

3.1 TTL NOR GATE

Electrical Specifications:

Operating frequency D.C. to 1 Mc/s

Operating temperature D.C. to 65° C

Input requirements:

	Voltage	Current
Input for logical 0 output	-3 to -6V	0.5 mA
Input for logical 1 output	0 to -.3 volts on all gate inputs.	

Output characteristics:

	Typical	Maximum
Delay time	400 nano seconds	450 nano seconds
Rise time	100 " "	130 " "
Storage time	160 " "	180 " "
Fall time	140 " "	140 " "

		Voltage	Current
Logic levels	Logical 1	-3 to -6V	0 to 3.0 mA
	Logical 0	0 to -.3V	0 to 0 mA

Noise immunity .1V

Power requirements:

	No load		Full load	
	Power	Current	Power	Current
-6V ± 5%	175 mW	25 mA	175 mW	25 mA

Load capabilities:

	FF	TRL NOR	ONE-SHOT	INVERTER	LAMP DRIVERS
No. of circuits it can drive at 55° C	4	4	4	4	10

Mechanical specifications:

Card identification	TRL/NOR
Card dimensions	11.5 cm x 16.5 cm
No. of connector pins	22
No. of gates per card	3- 2 input & 2- 4 input

3.2 FLIP-FLOP -

Electrical specifications:

Operating frequency	D.C. - 1 Mc/s
Operating temperature	0 - 55° C

Input requirements:

		Voltage	Current
Pulse - amplitude		-3.0V	0.5 mA
Level	(logical 1	0 to -.3V	0 mA
	logical 0	-3 to -6V	0.5 mA

Output characteristics:

		Typical	Maximum
Delay time		360 ns	400 ns
Rise time		20 ns	40 ns
Storage time		30 ns	40 ns
Fall time		300 ns	320 ns
		Voltage	Current
Logical levels	logical 0	0 to -.3V	0 mA
	logical 1	-3 to -6V	3.0 mA

Power requirements per card:

	No load		Full load	
	Power	Current	Power	Current
6V ± 5%	3 mW	.5 mA	3 mW	.5 mA
-6V ± 5%	140 mW	23.0 mA	180 mW	30.0 mA

Noise immunity 1V

Load capabilities:

	FF	TRL NOR	ONE-SHOT	INVERTER	LAMP DRIVERS
No. of circuits it can drive at 25° C	4	6	6	4	10

Mechanical specifications:

Card identification	Flip Flop
Card dimensions	11.5 cm x 16.5 cm
No. of connector pins	22
No. of circuits per card	2 Flip Flops & 2 inverters

3.3 ONE-SHOT MULTIVIBRATOR

Electrical specifications:

Operating frequency	D.C. to 1 Mc/s
Operating temperature	0 to 65° C

Input requirements:

		Voltage	Current
Pulse amplitude		3V	0.5 mA
Level	logical 0	0 to -0.3V	0 mA
	logical 1	-3.0 to -6.0V	0.5 mA
Noise immunity	1V		

Output characteristics:

	Typical	Maximum
Delay time	140 ns	180 ns
Rise time	40 ns	50 ns
Fall time	100 ns	130 ns
Level duration	0.3 μs(min.)	100 sec.

Logic levels	Voltage	Current
Logical 0	0 to -.3V	0 mA
Logical 1	-3V to -6V	0.5 mA

Power requirements:

	No load		Full load	
	Power	Current	Power	Current
+ 6V ± 5%	0.5 mW	0.08 mA	0.5 mW	0.08 mA
- 6V ± 5%	175.0 mW	29.5 mA	175.0 mW	29.5 mA

Load capabilities:

	FF	TRL NOR	ONE-SHOT	INVERTER	LAMP DRIVERS
No. of circuits it can drive at 25° C	4	4	4	4	10

3.4 INVERTER

Electrical specifications:

Operating frequency	D.C. to 1 Mc/s
Operating temperature	0 to 65° C

Input requirements:

	Voltage	Current
Logical 0 output	-3 to -6V	0.5 ma
Logical 1 output	0 to -0.3V	0 ma

Output characteristics:

	Voltage	Current
Logical 1 output	-3 to -6V	3.0 ma
Logical 0 output	0 to -0.3V	0 ma

	Typical	Maximum
Delay time	35 ns	50 ns
Rise time	15 ns	20 ns
Storage time	5 ns	10 ns
Fall time	15 ns	20 ns

Power requirements:

	No load		Full load	
	Power	Current	Power	Current
-6V ± 5%	280 mW	48 ma	280 mW	48 ma
+6V ± 5%	.3 mW	.05 ma	.3 mW	.05 ma

Noise immunity .75V

Load capabilities:

	FF	TRL NOR	ONE-SHOT	INVERTER	LAMP DRIVER
No. of circuits it can drive at 25° C	4	4	4	4	10

Mechanical specifications:

Card identification	Inverter
Card dimension	16.5 cm x 11.5 cm
No. of connector pins	22
No. of circuits per card	8

3.5 LAMP DRIVERS

Electrical specifications:

Operating frequency	0 to 10 Kc/s
Operating temperature	0 to 65° C

Input characteristics:

	Voltage	Current
Input voltage to light a lamp	-3 to -6V	25 uA
Maximum input voltage which will not light a lamp	1.5V	

Power requirements:

	Current	Power
-6V ± 5%	655 mA	3.95 W

Lamp specification:

Incandescent lamp	6V, 100 mA, 500 mW

Mechanical specifications:

Card identification	Lamp driver
Card dimensions	16.5 cm x 11.5 cm
No.of connector pins	22
No. of circuits per card	5

CHAPTER 4

PACKAGING

4.1 GENERAL

All circuits are to be packaged on printed circuit cards printed on copper clad sheets. Two types of copper clad sheets are available.

(1)	Single copper clad sheet	5-1/2" x 5-1/2"	
		copper thickness	.00135"
		Bakelite	1/16"
(2)	Double copper clad sheets	5-1/2" x 5-1/2"	
		copper thickness	.00135" x 2
		Bakelite	1/16"

Single copper clad sheets are cheaper but are more prone to warping. Here components can be mounted on one side only with printed connections on the other side, thus reducing component density on the card.

Double copper clad sheets are costlier but are less prone to warping. They permit greater flexibility in layout by permitting printing of circuits and mounting of components on both sides. The circuits can also be laid out in a nonplaner manner to a limited extent.

All resistances and capacitances have a 5% tolerance and a dissipation of 1/4 watt.

4.2 LAYOUT OF CARDS

The layout of cards are so arranged that as far as

possible supplies and earth always come to the same pins in all cards. One pin gap is maintained between supplies of opposite polarity and earth. To satisfy this requirement -6V collector supply is brought in at pin number 1 for all cards. +6V base bias supply is brought in at pin number 12 in all cards which use a base bias supply, the exceptions being the TRL gate card and lamp driver card, which do not use a base bias supply. The complementary supply pins, i.e., pin number 22 and pin number 11 are left spare so that if a card is inserted in a reverse manner by mistake, no circuit damage will result. Earth is brought in at pin No. 10 in all cards except in the TRL gate card where earth is brought in at pin No. 11. Since accidental plugging in of a TRL gate card into other sockets causes trouble, collector donnets here are made extra large for easy identification. In other cards the emitter donnet being one size smaller than collector and base donnets, according to usual convention.

Guide frames are not fixed on cards. The cards move in guide grooves made on a perspex bar fixed to the chasis. The amphenol connector is bolted to the chasis by two bolts at top and bottom and the cards slide into the connector through the guide groove. A plan and elevation of the card rack chasis is shown in Fig. 4.1.1. Provision of guide groove on perspex bar has the added advantage of permitting -6V collector supply to run close to the outer perimeter and still not run the risk of short circuiting the battery to the chasis. This ensures more efficient utilisation of available card area.

The card rack front cover can be opened and enough slack in cabling has to be given to permit it to fold out. This exposes the connector terminals and allows for testing and fault finding. Extension cards are provided for detailed tests.

In order to economise on the number of pins, separate test points have not been provided. However, transistors have been mounted with long leads so that oscilloscope probe can be directly attached to the transistor leads for testing and trouble shooting.

NOISE:-

Noise may be generated in many different ways. In digital equipment noise may originate from outside equipment because of

(1) electromagnetic radiation picked up by circuit acting as an aerial

(2) power supply and power line noise from other operating equipment.

These outside sources may be partially suppressed by shielding and filtering.

Noise may also originate within the digital equipment itself. Logic noise can be generated by fast switching of high currents on ground return busses particularly between logic cards. The resulting voltage drops developed across lead inductances can be amplified and propagated causing false transitions in gates triggering flip flops.

Low frequency power line noise is rejected by having large electrolytic bypass capacitors across power supply in

in power supply unit.

H.F. noise is rejected by having a 4700 pf ceramic capacitor across supply bus and earth on each card. Ceramic capacitors have better high frequency response than electrolytic capacitors.

Logic noise is reduced by running an earth bus in which circuits are connected to earth by as short leads as possible. This reduces lead inductances and skin effect and thus reduces logic noise.

4.3 T.R.L. GATE CARD

TRL/NOR/5-OF is a NOR gate card consisting of 5 NOR gates having three 2-input gates and two 4-input gates on each card. TRL gates use a transistor for each input. The maximum number of inputs for a gate is decided by the β_{min} of the transistor used. The 2N995 having a β_{min} of 35 allows a maximum fan-in of 4. Only three transistors are mounted on a 4-input gate converting it into a 3-input gate. A user requiring a 4-input gate can mount the 4th transistor and associated resistance.

The circuit diagram is shown in Fig. 4.3.1, the printed circuit in Fig. 4.3.2 and the card photograph is shown in Fig. 4.3.3. The description of the pins is given below. The gates are numbered as shown in Fig. 3.1.

Pin No.	Description	Pin No.	Description
1	-6V collector supply	2	input 1 to NOR Gate1
3	input 2 to NOR Gate 1	4	" 1 " 2

Pin No.	Description	Pin No.	Description
5	input 2 to NOR Gate 2	6	input 1 to NOR Gate 3
7	" 2 " 3	8	output of NOR Gate 3
9	output of " 2	10	" " " 1
11	Earth	12	output " " 4
13	output of " 5	14	input 1 " " 5
15	input 2 of " 5	16	" 3 " " 5
17	" 2 of " 5	18	" 1 " " 4
19	" 2 of " 4	20	" 3 " " 4
21	" 4 of " 4	22	spare

Since the NOR is an universal function which is logically complete conjunction (AND) and disjunction (OR) functions have not been provided.

4.4 INVERTER

INV-8-OF is a card consisting of 8 inverters. Each inverter has a fan-out of 4. The presence of speed up capacitors reduces the storage time to negligible amount and the only parameters in the transient characteristics which are of importance are the rise and fall times. The inverters are named as shown in Fig. 3.4. The photograph of the printed circuit is given in Fig. 4.4.2 and the circuit diagram in Fig. 4.4.1. The card photograph is shown in Fig. 4.4.3. The pin connections for the card are listed below.

Pin No.	Description	Pin No.	Description
1	-6V collector supply	2	input to inverter 3
3	input to inverter 2	4	" " " 1
5	" " " 4	6	output of " 4
7	output of " 3	8	" " " 2
9	" " " 1	10	Earth
11	spare	12	+6V base bias supply
13	"	14	Output of inverter 3
15	output of inverter 6	16	" " " 7
17	" " " 8	18	input " " 8
19	input " " 5	20	" " " 6
21	" " " 7	22	spare

4.5 FLIP FLOP

Two flip flops and two inverters are mounted on each card and they are numbered as shown in Fig. 3.2. The inverter provides a 180 ns delay and can be used when the cards are to be used as shift registers. The inverter components are not mounted on the card and will have to be mounted by the user. Each flip flop is provided with 5 inputs, namely, DC-set and reset, pulse-set and reset, and trigger, but the associated components of input circuit are not mounted on cards. If a user wants to use the circuit as a SR flip flop the associated input terminal components will have to be mounted. Whereas if a flip flop is to be used as a binary (in counter applications) only components associated with trigger terminal need be mounted. The present design thus permits a wide flexibility in the utility

of the flip flop. The circuit diagram is shown in Fig. 4.5.1, printed circuit in Fig. 4.5.2, and the card photograph in Fig. 4.5.3. The pin connections are listed below:

Pin No.	Description	Pin No.	Description
1	6V collector supply	2	output of inverter 1
3	D.C. set FF 1	4	output FF 1
5	pulse set FF 1	6	complementary output FF 1
7	trigger FF 1	8	D.C. reset FF 1
9	pulse reset FF 1	10	earth
11	spare	12	+6V base bias supply
13	spare	14	pulse set FF 2
15	D.C. reset FF 2	16	trigger FF 2
17	complementary output FF 2	18	pulse set FF 2
19	output FF 2	20	D.C. set FF 2
21	output inverter 2	22	spare

4.6 MONOSTABLE MULTIVIBRATOR

4 one-shots are located in one card and are numbered according to Fig. 3.3. The one-shots are so arranged so as to provide a delay depending on the RC constants. The one-shot is triggered by a negative going edge or the leading edge of the input pulse and provides an output pulse determined by C_D and R_D. The relationship between C_D R_D and the delay is given in section 7.4.1. In order to provide a delay two monostables are connected in cascade in which the trailing monostable is triggered by the complementary output of the leading monostable. The leading monostable provides the delay and the

trailing monostable is used as a pulse shaper giving the pulse width. For example, if we want a 1 μs pulse delayed by 5 μs, the leading one-shot C_D is adjusted to give a 5 μs delay and is triggered by the input pulse. The complementary output of this stage is used to trigger the trailing one-shot. The complementary output will have a falling edge on the trailing end and this will trigger the trailing one-shot, in which C_D is adjusted to give a 1 μs pulse. In a card the input is connected to one-shot 1 or 3. The complementary output of these two one-shots can be connected to one-shot 2 and 4 by connectors within the card and these are adjusted to give required pulse width. If a one-shot card is to be used as a delay unit, one-shot 1 and 3 on the card provide delays, and one-shot 2 and 4 provide required output pulse width.

The circuit diagram is shown in Fig. 4.6.1, printed circuit in Fig. 4.6.2 and the card photograph in Fig. 4.6.3. The pin connections for the one-shot are as follows:

Pin No.	Description	Pin No.	Description
1	-6V collector supply	2	output of OS 2
3	complementary output OS 2	4	input OS 2
5	output OS 1	6	complementary output OS 1
7	input OS 1	8	spare
9	spare	10	earth
11	spare	12	+6V base bias supply
13	spare	14	spare
15	spare	16	input OS 3
17	complementary output OS 3	18	output OS 3
19	input OS 4	20	complementary output OS 4
21	output OS 4	22	spare

4.7 LAMP DRIVERS

Five lamp drivers are located in one card and are numbered as in Fig. 3.5. In order to have negligible loading effect the lamp driver is connected in the Darlington fashion. The transistor in the final stage is a AC128 (a power transistor). Though from considerations of speed a slow transistor like 2N404 can suffice for the driver stage, 2N995 has been preferred from considerations of I_{cbo}. The 2N404 has a high I_{cbo} and can switch on the lamp for a '0' at high temperatures. The lamp is connected in series with the collector of the output stage. There are two output terminals and one input terminal for each stage. A 6V 135 mA bulb is connected across the output terminals and the lamp is located in the consul display unit. The input terminal is connected to the flip flop output to be displayed. The lamp lights for the '1' state of the FF.

The lamp drivers require 3.95 watts of power per card and it is uneconomical to supply such large quantities of power from the main regulated supply. As these lamp drivers permit a wide flexibility in the voltage supplies, they are supplied power from a separate power supply unit with poor regulation but large current capability.

The circuit diagram for the lamp driver card is given in Fig. 4.7.1, printed circuit in Fig. 4.7.2 and card photograph in Fig. 4.7.3. The pin connections are listed below:

Pin No.	Description	Pin No.	Description
1	-6V collector supply	2	terminal 1 lamp 1
3	terminal 2 lamp 1	4	input for lamp 1
5	" 1 " 2	6	terminal 2 lamp 2
7	input for lamp 2	8	spare
9	spare	10	earth
11	spare	12	spare
13	input for lamp 3	14	terminal 1 lamp 3
15	terminal 2 lamp 3	16	input for lamp 4
17	" 2 " 4	18	terminal 1 lamp 4
19	input for lamp 5	20	" 1 " 5
21	terminal 2 lamp 5	22	spare

REFERENCES FOR CHAPTER 5

1. Motorola High Speed Switching Transistor Handbook 1963, published by Motorola Incorporated.

2. Design of Transistorized Circuits for Digital Computer by Abraham I. Pressman, John Rider Publication, 1959.

CHAPTER 5

DESIGN PROCEDURES

5.1 PRELIMINARY DESIGN

5.1.1 TRL Gates:

In Fig. 5.1.1 when all transistors are cut off the output voltage cannot fall below -3V after delivering a load current of 3 mA. This sets an upper limit for R_C neglecting leakage currents

$$R_C = \frac{6 - 3}{3} = 1K\Omega$$

Consider when only one transistor is conducting and remaining others are cut off I_{cc0} = current through collector resistor when output is a '0', neglecting V_{ces}

$$I_{cc0} = 6/1 = 6 \text{ mA}$$

This is the collector current of ON transistor.

I_b = base current required to saturate transistor

= 6/15 = 4 mA (assuming $\beta_F = 15$ for saturation.)

$$R_B = \frac{3 - .7}{4} = \frac{2.3}{4} = 5.75K\Omega$$

where -3V = input voltage

-.7V = V_{bes} for transistor under saturation.

Preliminary design figures:- In Fig. 5.1.1 $R_C = 1K\Omega$, $R_B = 5.75K\Omega$

5.1.2 Inverter:

In Fig. 5.1.2 at full load the output voltage must not fall below -3V while supplying full load of 3 mA neglecting

leakage current.

$$R_C = \frac{6 - 3}{3} = 1K\,\Omega$$

when the transistor is ON neglecting V_{ces}

$$I_{cc1} = 6/1 = 6 \text{ mA.}$$

$$I_b = 6/15 = .4 \text{ mA} \quad (\text{assuming } {}_F = 15 \text{ for saturation}).$$

$$R_K = \frac{V_1 - V_{bes}}{I_b} = \frac{2.3}{.4} = 5.7K\,\Omega$$

when transistor is OFF $V_{ob} = .1V$

current through $R_K = I_k = .4/5.7 = .0705$ mA

$$R_B = \frac{6 - .1}{.0705} = 82K\,\Omega$$

The base bias supply is connected to earth through two identical resistances (R_B) in the form of a voltage divider. The centre point is connected to the base terminal. This ensures that in the absence of an input, the +6V supply which exceeds V_{ebo} of 2N995 will not reach the base in full magnitude.

Preliminary design figures in Fig. 5.1.2 are $R_C = 1K\,\Omega$, $R_K = 5.7K\,\Omega$, $R_B = 82K\,\Omega$, $C_K = 82$ pf.

5.1.3 Flip Flop:

In Fig. 5.1.3 consider Q_1 ON and Q_2 OFF. R_C must be chosen to allow a 3 mA load to be drawn at A without the voltage at A falling below -3V.

$$R_C = \frac{6 - 3}{3.4} = 880\,\Omega$$

This allows for .4 mA base drive for saturating Q_1.

$$R_K = \frac{3 - .7}{.4} = 5.7K\,\Omega$$

To maintain Q_2 OFF the voltage at its base should be +.1V and base current = I_{ko}.

$$I_{ko} = \frac{.4}{5.7} = .0705 \text{ mA}$$

This current must come from the V_{bb} R_B source.

$$R_B = \frac{5.9}{.0705} = 84K\,\Omega$$ (neglecting base leakage current).

Operating frequency = 1000 Kc/s, time period = 1/1000 = 1 μs.

Time constant C_TR_T must be at least 5% of T, C_TR_T = .2 μs.

Select R_T = 4.7K Ω , $C_T = \frac{.2 \times 10^{-6}}{4.7 \times 10^3}$ = 42.6 pf.

Select C_T = 56 pf, C_TR_T = .254 μs. This is within limits.

R_P must not load the trigger source but in combination with C_PR_P must permit complete discharge of C_P in one time period. Select C_P = 82 pf, R_P = 10K Ω.

C_PR_P = .82 μs. This is within limits.

Preliminary design figures for flip flop are R_C = 880 Ω, R_K = 5.7K Ω , R_B = 84K Ω, R_T = 4.7K Ω , R_P = 10K Ω, R_A = 4.7K Ω, C_T = 56pf, C_P = 82pf , C_K = 56pf where R_i's and C_i's are defined in Fig. 5.1.3.

5.1.4 Monostable Multivibrator:

In Fig. 5.1.4 consider Q_1 ON and Q_2 OFF. A bse base drive of .4 mA is required to saturate Q_1.

$$R_C = \frac{6 - 3}{3.4} = 880\Omega$$

$$R_K = \frac{3 - .7}{.4} = 5.75K\Omega$$

when Q_1 is OFF a reverse bias of + .1V must be maintained at the base, neglecting base leakage current, current through $R_K = I_k$

$$I_k = \frac{.4}{5.75} = .0705 \text{ mA}$$

$$R_B = \frac{6 - .1}{.0705} = 84K\Omega$$

V_{ebo} = 4V. Hence $V_s^* = .9 \times 4 = 3.6V$

Voltage across $C_D = \frac{V_{cc} \times R_T}{R_P + R_T} = 3.6V$

Therefore, $R_T = 1.5\ R_P$.

$I_b = .4$ mA

$I_c = .4 \times \beta_F = .4 \times 20 = 8$ mA

$R_P = 6/8 = 750\Omega$ neglecting V_{ces}

$R_T = 1.5 \times 750 = 1.15K\Omega$

C_D and R_D are adjusted to give required delay.

Design figures are given below according to Fig. 5.1.4,

$R_C = 880\Omega$, $R_K = 5.75K\Omega$, $R_B = 84K\Omega$, $R_P = 750\Omega$,

$R_T = 1.15K\Omega$, $R_I = 10K\Omega$, $C_I = 470$ pf.

5.1.5 Lamp Driver:

Consider Fig. 5.1.5; current required to drive lamp = 100 mA. Hence $R_E = 6/100 = 60\,\Omega$.

Lamp resistance = $20\,\Omega$. Hence $R_C = 60 - 20 = 40\,\Omega$

Base drive for $Q_2 = 5/100 = .05$ mA.

$$R_B = \frac{3 - .7}{.057} = 46K\,\Omega$$

Preliminary design figures in Fig. 5.1.5 are $R_C = 40\,\Omega$, $R_B = 46K\,\Omega$, lamp 6V, 135 mA, 250 mW.

The requirement for this circuit is that we must use a high transistor for the driver stage, i.e., Q_2.

5.2 CONSIDERATIONS FOR WORST CASE DESIGN

In designing digital circuits it is necessary to take into account worst conditions that can be reasonably expected. Deviations from the ideal condition may be due to tolerances of the circuit components and to external influences such as varying supplies, loads and environmental conditions.

The parameters to be considered may be divided into the following groups

(1) Parameters which can be chosen by the designer such as nominal values of components and supply voltages.

(2) Parameters which are fixed once the choice of components has been made, for example, the current amplification factor of transistor, junction voltages, component tolerances and maximum permissible dissipation.

(3) Parameters which are fixed by the requirements of the system in which the unit is used, e.g., fan-in, fan-out noise, ambient temperature, etc.

A necessary condition to be satisfied in all cases is that the circuit must function satisfactorily.

If each varying parameter is associated with an axis of a multidimensional space, the circuit for any given value of parameter will be a point in this space. Each variation in a parameter moves the point and one can think of a multidimensional volume within which the circuit should operate satisfactorily. The designer aims to fix the point corresponding to nominal values to obtain maximum reliability. The concept is simple but very difficult to implement. Only absolute worst case (i.e., when all parameters change in a way to deteriorate the performance) is examined for satisfactory performance.

One of the serious problems to be handled in design of logic circuits is noise. Under the influence of noise, circuit tends to produce false output, e.g., the base to emitter voltage of an inverting transistor in the OFF state is liable to increase resulting in a wrong output (though momentarily). Noise can also appear on the supply lines (especially if the decoupling is not good) and one has to modify the design values of supply for worst case analysis. The design values V^* and $\underline{V}$ are derived as follows:

V = nominal supply voltage

n_p = power supply tolerance

N = noise present in supply

V^* = maximum supply voltage = $V (1 + n_p) + N$

$\underline{V}$ = minimum supply voltage = $V (1 - n_p) - N$

The following circuits are being designed using the worst case design philosophy:

(1) TRL NOR Gate

(2) Inverter

(3) Flip Flop

(4) One-shot

(5) Lamp driver

5.3 GENERAL CONSIDERATIONS

Choice of Logic Levels:

In normal practice the choice of transistor is governed by system parameters like logic levels, loading considerations, etc. In India, however, there are only a limited number of switching transistors and hence a transistor is first selected of the basis of Chapter 2 and system needs are tailored to suit transistor chosen.

Voltage levels of system	Min	Max
V_0	0	-.3V
V_1	-3V	-6.3V

Choice of Collector Supply Voltage:

The power supply dissipation in R_C sets an upper limit

on the choice of V_{cc} and R_C.

$$P_D = \text{power dissipation in } R_C = I_{cc0} \times V_{cc} = \gamma I_{cc1} V_{cc} = \frac{NR(1+n_p) I_{cc1} V_{cc}}{1 - n_p - V_1/V_{cc}}$$

$$= \frac{a x}{\frac{1}{V_1}(b - 1/x)}$$

where $a = NR (1+n_p) I_{cc1}$

$b = 1 - n_p$

$$\frac{dP_D}{dx} = \frac{(bx-1) V_1 ax - V_1 ax^2 b}{(bx-1)^2} = 0 \quad \text{for minimum } P_D$$

$$(bx-1) 2V_1 ax - V_1 ax^2 b = 0. \quad \text{Hence} \quad x = 2/b$$

$$\frac{V_{cc}}{V_1} = \frac{2}{1-n_p} = 2$$

$$V_{cc} = 2 \times V_1 = 6 \text{ volts.}$$

<u>Transistor parameters</u>:

Collector saturation voltage = V_{ces} = -.3V

Base " " = V_{bes} = -.7V

Min. bias to cut off transistor = V_{ob} = +.1V

Collector leakage current I_{c1}* = .0025 mA

Base leakage current I_{b1}* = .0025 mA

Minimal β 35

Forced to ensure saturation (β_F) = 20.

Available supply voltages:

	Nominal	Maximum	Minimum
Collector supply	-6V	-6.3V	-5.7V
Base bias supply	+6V	+6.3V	+5.7V

Temperature:

Maximum	Ambient	Minimum
70° C	25° C	0° C

Tolerances:

Tolerances for resistances $n_R = .05$

" " capacitances $n_C = .05$

" " power supply $n_p = .05$

5.4 TRL NOR GATE

D.C. Conditions:

The avilable output current for a given gate must be equal to or greater than the maximum current required to drive subsequent circuits.

The spread in V_{be} versus I_b characteristics must be sufficiently small to ensure reasonably uniform base drives to transistors with parallel inputs.

There must be sufficient voltage margin between V_{ces} of ON transistor and V_1 the minimum voltage at OFF collector to ensure two unambiguous stable states.

Let V_{cc} = negative collector supply voltage

V_1 = minimum output voltage for a 1

I_b = minimum base current to ensure transistors in saturation.

Refer to Fig. 5.4.1, writing the nodal equation at A

$$I_{cc1} = \sum I_b + I_{c1}$$

$$\frac{V_{cc} - V_1}{R_C} = NI_b + M I_{c1} \qquad 5.4.1$$

Summing the voltage between earth and A

$$V_1 = V_{bes} + \underline{I}_b \underline{R}_B \qquad 5.4.2$$

Writing the nodal equation at A in Fig. 5.4.2,

$$\frac{V_{cc} - V_{ces}}{R_C} = I_c + (N-1) I_{c1} - M I_{b1} \qquad 5.4.3$$

Writing the nodal equation at A in Fig. 5.4.3, when all transistors are conducting

$$\frac{V_{cc} - V_{ces}}{R_C} = MI_c - NI_{b1} \qquad 5.4.4$$

Design procedure for TRL Gates:

Specifications:

	Available				Required			
	input volts		input current		output volts		output current	
	Min	Max	Min	Max	Min	Max	Min	Max
V_0	0	-.3V	0	0	0	-.3V	0	0
V_1	-3V	-6.3V	.5mA	.5mA	-3.0	-6.3	0	3.0mA

Estimation of R_C:

As we are permitting a maximum load current of 3 mA, i.e., in equation 5.4.1, MI_b term is 3 mA substituting this in equation 5.4.1

$$R_C = \frac{V_{cc} - V_1}{MI_b + MI^*_{c1}} = 910\ \Omega$$

Estimation of I^*_c:

Substituting R_C in equation 5.4.3,

$$\frac{V^*_{cc} - V_{ces}}{R_C} = I^*_c + (N-1)\, I_{c1} - MI_{b1}$$

$$I^*_c = 6.95 \text{ mA}$$

Estimation of I_c from equation 5.4.4:

$$I_c = \frac{1}{M} \frac{V_{cc} - V_{ces}}{R_C} + MI_{b1}$$

$$I_c = 1.74 \text{ mA}$$

Hence from the two values of I_c,

$$I^*_c = 6.95 \text{ mA}$$

$$I_b = \frac{6.95}{15} = .465 \text{ mA}$$

Substituting in equation 5.4.2

$$R_B = \frac{V_1 - V_{bes}}{I_b} = 4.7K\ \Omega$$

Hence designed values in Fig. 5.1.1 are $R_C = 910\ \Omega$, $R_B = 4.7K\ \Omega$.

5.5 INVERTER

The function of the inverter is to invert the polarity of an input signal producing a compatible output. It also provides power gain and pulse shape restoration. In Fig. 5.5.1, when input voltage is '1' current flow through R_K overcoming the current through the base bias source (V_{bb} R_B) and drives the transistor in saturation. The output voltage in such a case is '0' ($-V_{ces}$). When the input voltage is '0' ., current through the V_{bb} R_B source flows through R_K and reverse biasses the transistor. The output in this case is '1' ($-V_1$), and current through the V_{cc} R_C source flows into the load. The design must ensure that the drop in R_C due to load current flow does not let the level fall below -3V. R_K is chosen to ensure that with -3V input voltage, the transistor is driven into saturation. R_B is chosen to ensure reverse bias to cut off transistor under worst conditions of leakage current with an input voltage of -3V.

Choice of R_C:

Collector resistor R_C can be chosen by analysing the output circuit. Replace the transistor by a current generator during OFF state as shown in Fig. 5.5.2a, The conditions during ON state are shown in Fig. 5.5.2b. Writing the nodal equation at A in Fig. 5.5.2a

$$R_C^* = \frac{V_{cc} - V_1}{I_{c1} + I_{L_1}} \qquad 5.5.1$$

Writing the nodal equation at A in Fig. 5.5.2b

$$\underline{R}_C = \frac{V^*_{cc} - \underline{V}_O}{I^*_c + I^*_{LO}} \qquad 5.5.2$$

Ratio of collector current to load current:

$$NR = \frac{R^*_C}{\underline{R}_C} = \frac{(1 + n_R)}{(1 - n_R)} \frac{R_C}{R_C} \qquad 5.5.3$$

using these relationships equations 5.5.1 and 5.5.2 may be rewritten as

$$(1 + n_R) R_C = \frac{(1 - n_P) V_{cc} - V_1}{\underline{I}_{cc1}}$$

where I_{cc1} = current through R_C when output is 1.

I_{cc0} = " " " " " " 0.

In equation 5.5.1 assuming $\underline{V}_O = 0$ we have

$$I^*_c + I^*_{LO} = \frac{(1 + n_P) V_{cc}}{(1 - n_R) R_C}$$

$$y = \frac{I^*_{cc0}}{I_{cc1}} = \frac{NR (1 + n_P)}{1 - n_P - (\underline{V}_1 / V_{cc})} \qquad 5.5.4$$

Input network:

The synthesis equations for the input network can be written from Figs. 5.5.3 and 5.5.4.

Writing the nodal equation at A in Fig. 5.5.4

$$\frac{\underline{V}_{ob} + V^*_O}{R_K(1+n_R)} - \frac{V^*_{bb} - \underline{V}_{ob}}{R_B(1+n_R)} + \frac{\underline{V}_{ob}}{R_B(1+n_R)} + I_{b1} = 0 \qquad 5.5.5$$

Writing the nodal equation at B in Fig. 5.5.3

$$\frac{V_{-1} - V^*_{bes}}{R_K(1+n_R)} - \frac{V^*_{bb} + V_{bes}}{R_B(1-n_R)} - \frac{V^*_{bes}}{R_B(1+n_R)} - I_b = 0 \qquad 5.5.6$$

Equations 5.5.5 and 5.5.6 are solved simultaneous to given R_B and R_K.

Design procedure:

Specifications

	Available				Required			
	Input volt		Input current		Output volt		Output current	
	Min	Max	Min	Max	Min	Max	Min	Max
V_0	0	-0.3V	0	.0025mA	0	-0.3V	0	.0025mA
V_1	-3V	-6.3V	.5mA	.5mA	-3V	-6.3V	0	3.0 mA

Estimate of current through R_C:

$$I_{cc1} = I^*_{L1} + I^*_{c1} = 3.025 \text{ mA}$$

Selection of transistor:

2N995 silicon Epitaxial planar PNP transistor is chosen as discussed in Chapter 2.

Estimation of R_C:

R_C is calculated from equation 5.5.2

$$R_C = \frac{V_{cc} - V_1}{I_{cc1}} = \frac{5.7 - 3.0}{3.025 \times 1.05} = 850\,\Omega$$

Select $R_C = 820\,\Omega$

Estimation of maximum collector current:

Calculate I_c^* from equation 5.5.2

$$I_c^* = \frac{V_{cc}^* - V_{-0}}{R_C} + I_{LO} = \frac{6.3 - 0}{820 \times 9.5} + 0 = 8.1 \text{mA}$$

$$I_{-b} = \frac{I_c^*}{\beta_F} = \frac{8.1}{20} = .4054 \text{ mA}$$

Calculation of input parameters R_K and R_B :

Calculate R_K and R_B from equations 5.5.5 and 5.5.6

$$\frac{V_{-ob} + V_0^*}{R_K(1-n_R)} - \frac{V_{bb} - V_{-ob}}{R_B(1+n_R)} + \frac{V_{-ob}}{R_B(1+n_R)} + I_{b1} = 0$$

$$\frac{.1 + .2}{.95\ R_K} - \frac{5.7 - .1}{1.05\ R_B} + \frac{.1}{1.05\ R_B} + .0025 = 0$$

$$\frac{1}{R_K} = \frac{1}{.316}\left[-.0025 + \frac{5.25}{R_B}\right] \qquad 5.5.7$$

Rewriting equation 5.5.6

$$\frac{V_{-1} - V_{bes}}{(1+n_R)\ R_K} - \frac{V_{bb} + V_{bes}^*}{(1-n_R)\ R_B} - \frac{V_{bes}^*}{(1-n_R)R_B} - I_b = 0$$

$$\frac{3 - .6}{1.05\ R_K} - \frac{6.3 + .6}{.95\ R_B} - \frac{.6}{.95\ R_B} = .405$$

$$\frac{2.28}{R_K} - \frac{7.9}{R_B} = .405 \qquad 5.5.8$$

substituting for R_K in equation 5.5.8

$$\frac{2.28}{.316}\left[\frac{5.25}{R_B} - .0025\right] - \frac{7.9}{R_B} = .405 \text{ mA}$$

$$R_B = \frac{30.1}{.423} = 72 \text{ K}\Omega, \quad \text{selected } R_B = 75\text{K}\Omega.$$

substitute R_B in equation 5.5.8

$$\frac{2.28}{R_K} - \frac{7.9}{R_B} = .405$$

$$R_K = \frac{2.28}{.51} = 4.6\text{K}\Omega \quad \text{Hence select } R_K = 4.7\text{K}\Omega$$

Designed values for inverter in Fig. 5.5.1 are $R_C = 820$, $R_K = 4.7\text{K}\Omega$, $R_B = 75\text{K}\Omega$, $C_K = 56$ pf.

5.6 FLIP FLOP

A basic flip flop is shown in Fig. 5.6.1. It has two stable states (i) Q_1 OFF and Q_2 ON (ii) Q_1 ON and Q_2 OFF. A reliable flip flop must fulfil the following conditions under worst case combination of component and power supply variation.

1. The flip flop must continue to remain in a stable state unless triggered. To ensure this R_K and R_B must be chosen so that when one side is ON the other side is OFF, and at the same time, the output voltage of the OFF side allows sufficient base drive to saturate ON side.
2. The output voltage must be compatible under worst conditions of loading.

3. The flip flop must change state within a prescribed time after the application of the trigger pulse.

The analysis is started by assuming one stable state. It is assumed that Q_1 is ON and Q_2 is OFF. Fig. 5.6.2 shows conditions of currents and voltages with Q_1 ON and Q_2 OFF.

Writing the nodal equations at A in Fig. 5.6.2

$$\frac{V_{ob} + V^*_{ces}}{R_K} - \frac{V_{bb} - V_{ob}}{R^*_B} + I_{b1} = 0 \qquad 5.6.1$$

Writing the nodal equations at B in Fig. 5.6.2

$$\frac{V_1 - V^*_{bes}}{R^*_K} - \frac{V^*_{bb} + V^*_{bes}}{R_B} - I_b = 0 \qquad 5.6.2$$

Writing the nodal equations at C in Fig. 5.6.3

$$\frac{V_{cc} - V_1}{R^*_C} - \frac{V_1 - V_{bes}}{R^*_K} - I^*_{c1} - I^*_{L_1} = 0 \qquad 5.6.3$$

Equations 5.6.1, 5.6.2 and 5.6.3 are solved simultaneously in the form of a matrix to yield the unknown values of R_C, R_B and R_K but for this, one will have to guess the transistor characteristics. In the present case the problem does not arise because the transistor is already chosen but the standard procedure would be to estimate collector current and then select transistor from it. The transistor parameters can now be substituted in equations 5.6.1, 5.6.2 and 5.6.3 to yield R_C, R_B and R_K.

Estimation of collector current:

I_c^* = maximum collector current for ON transistor

I_b = minimum base current for ON transistor.

$$I_b = \frac{I_c^*}{-F} = \frac{V_{cc}^*}{R_C\ -F} + \frac{I_O}{-F}$$

From equation 5.5.4

$$y = \frac{NR\ (1 + n_p)}{1 - n_p - V_1/V_{cc}} = \frac{I_c^* - I_O^*}{I_{cc1}}$$

where
From Fig. 5.6.2

$$I_{cc1} = I_{L_1} + I_{k1} + I_{c1}$$

$$I_{k1} = I_b^* + I_{s2}^*$$

as I_s is always less than I_b

$$I_{k1}^* = 2I_b^* = \frac{2I_c^*}{\beta_{-F}} \text{ is an optimistic error.}$$

Hence $I_{cc1} = I_{L1}^* + 2I_c^*/\beta_F^*$

$$y = \frac{I_c^* - I_O^*}{I_{cc1}} = \frac{I_c^* - I_O^*}{I_{L1}^* + (2I_c^*/\beta_F^*)}$$

Cross multiplying and separating I_c^*

$$I_c^* = (I_{L1}^* + I_O^*) / (1 - (2\ y/\ _F^*)) \qquad 5.6.4$$

To check that V_1 does not fall below the prescribed limits, V_1 is calculated from the remaining parameters under conditions of maximum loading.

$$\underline{V}_1 = \frac{V^*_{cc} \; R^*_K + V^*_{bes} \; \underline{R}_C - I^*_{L1} \; \underline{R}_C \; R^*_K}{R^*_K + \underline{R}_C} \qquad 5.6.5$$

For finding the maximum stored charge I^*_b must be determined.

$$I^*_b = \frac{V^*_1 - \underline{V}_{bes}}{\underline{R}_K} - \frac{\underline{V}_{bb} - \underline{V}_{bes}}{R^*_B} \qquad 5.6.6$$

To ensure reverse bias for OFF transistor, V^*_{ob} is calculated.

$$V^*_{ob} = \frac{V^*_{bb} \; R^*_K}{R^*_K + \underline{R}_B} \qquad 5.6.7$$

Design procedure:

Specifications:

	Required Input				Available Input			
	Volt		Current		Volt		Current	
	min	max	min	max	min	max	min	max
V_0	0	-.3V	0	.0025mA	0	-.3V	0	0
V_1	-3	-6.3V	.5mA	.5 mA	-3V	-6.3V	0	3.0 mA

Estimation of I^*_c:

$$y = \left[\frac{1 + n_R}{1 - n_R}\right]\left[\frac{1 + n_P}{1 - n_P - V_1/V_{cc}}\right] = \frac{1.05}{.95} \times \frac{1.05}{1 - .05 - .5} = 2.58$$

$$I^*_c = \frac{yI_1 + I^*_0}{1 - \frac{2y}{\beta^*_F}} = \frac{2.58 \times 3 + 0}{1 - \frac{2 \times 2.50}{20}} = 10.5 \text{ mA}$$

Selection of transistor :- 2N995 is selected and its pertinent parameters are

$$V^*_{ces} = -0.2V$$

$$V^*_{bes} = -0.7\ V$$

$$\beta^*_F = 20$$

Calculation of R_K, R_B and R_C:

Unknown resistances R_K, R_B and R_C can be found by solving equations 5.6.1, 5.6.2 and 5.6.3. Rewriting the same in matrix form

$$\frac{K_{11}}{R_C} + \frac{K_{12}}{RR_K} + \frac{K_{13}}{R_B} = A_1 \qquad 5.6.8$$

$$\frac{K_{21}}{R_C} + \frac{K_{22}}{R_K} + \frac{K_{23}}{R_B} = A_2 \qquad 5.6.9$$

$$\frac{K_{31}}{R_C} + \frac{K_{32}}{R_K} + \frac{K_{33}}{R_B} = A_3 \qquad 5.6.10$$

$$K_{11} = \frac{V_{cc}\,(1 - n_P) - V_{-1}}{1 + n_R} = \frac{5.7 - 3}{1.05} = 2.57$$

$$K_{12} = -\frac{V_{-1}}{1 - n_R} = \frac{-3}{.95} = -3.16$$

$$K_{13} = 0$$

$$K_{21} = 0$$

$$K_{22} = \frac{V^*_{ces} + V_{-ob}}{1 - n_R} = -\frac{.2 + .1}{.95} = -.316$$

$$K_{23} = \frac{V_{bb}(1 - n_P) - V_{-ob}}{1 + n_R} = \frac{5.7 - .1}{1.05} = 5.32$$

$$K_{31} = \frac{V_{cc}(1 + n_P)}{\beta_F (1 - n_R)} = \frac{6.3}{20 \times .95} = .330$$

$$K_{33} = \frac{V^*_{bes} + V_{bb}(1 + n_P)}{1 - n_R} = \frac{6.9}{.95} = 7.3$$

$$K_{32} = \frac{-(V_1 - V^*_{bes})}{1 + n_R} = -2.4/1.05 = -2.3$$

$$A_1 = I_{l1} + I_{c1} = 3 + .0025 = 3.0025 \text{ mA}$$

$$A_2 = I_{b1} = .00256$$

$$A_3 = 0$$

Substituting $K_{i's}$ in equation 5.6.8 we have

$$1/R_C = (1/2.57)\ (3.00256 + (3.16/R_K)) \qquad 5.6.11$$

Substituting $K_{i's}$ in equation 5.6.9 we have

$$1/R_B = (1/5.34)\ (.00256 + (.316/R_K)) \qquad 5.6.12$$

Substituting $K_{i's}$ in equation 5.6.10 we have

$$.33/R_C - 2.29/R_K + 7.3/R_B = 0$$

Substituting for $1/R_B$ and $1/R_C$ we have

$$\frac{.33}{2.57}\left(3.00256 + \frac{3.16}{R_K}\right) - \frac{2.29}{R_K} + \frac{7.25}{5.34}\left(.00256 + \frac{.316}{R_K}\right) = 0$$

Hence $R_K = 1.464/.3456 = 43K\Omega$

$R_K = 4.7K\Omega$ is selected.

Substituting value of R_K in equation 5.6.11

$1/R_C = (1/2.57)\ (3.00256 + (3.16/4.7))$. Therefore, $R_C = 720$

Therefore, $R_C = 820\ \Omega$ is selected.

Substituting R_K in equation 5.6.12

$1/R_B = (1/5.34)\ (.00256 + (.316/4.7))$. Hence $R_B = 76K\Omega$

Therefore, $R_B = 75K\Omega$ is selected.

To check for $\underline{V}_1$ under full loading conditions from equation 5.6.5

$$\underline{V}_1 = \frac{V^*_{cc}\ R^*_K + V^*_{bes}\ \underline{R}_C - \underline{I}_{L1}\ \underline{R}_C\ R^*_K}{R^*_K + \underline{R}_C}$$

$$= \frac{6.3x1.05x4.7 + .7x.95x.82 - 3x.95x.82x1.05x4.7}{1.05x4.7 + .95x.82} = -3.52$$

This satisfies our specification of a minimum of -3V.

To check if maximum reverse bias is within limits, V^*_{ob} is calculated from equation 5.6.7

$$V^*_{ob} = \frac{V^*_{bb}\ R^*_K}{R^*_K + \underline{R}_B} = \frac{6.3 \times 1.05 \times 4.7}{1.05 \times 4.7 + .95x75} = .41V$$

This is within limits of 2N995 and sufficient to reverse bias the transistor.

I_b^* is calculated from equation 5.6.6

$$I_b^* = (V_1^* - V_{-bes})/R_{-K} - (V_{-bb} - V_{-bes})/R_b^*$$

$$\frac{3 - .7}{1.05 \times 4.7} - \frac{5.7 - .7}{1.05 \times 75} = .4020 \text{ mA}$$

$$I_c^* = \frac{6.3}{.95 \times 820} = 7.95 \text{ mA}$$

$$I_{-b} = \frac{7.95}{20} = .3970 \text{ mA}$$

Hence I_b of .402 mA is sufficient to saturate transistor.

Input circuit:

Operating frequency = 1000 Kc/s

$$T = 1/500 \times 10^3 = 1 \ \mu s$$

The time constant $C_T R_T$ as shown in Fig. 5.6.1, must be so chosen that it is approximately one fifth of T, i.e., $C_T R_T = T/5$. Hence $C_T R_T = 1/5 = .2 \ \mu s$. Select $R_T = 4.7K\Omega$.

$$C_T = .2 \times 10^{-6} / 4.7 \times 10^3 = 42.5 \times 10^{-12} F.$$

Select $C_T = 56$ pf

$$C_T R_T = 56 \times 10^{-12} \times 4.7 \times 10^3 = .264 \ \mu s,$$

and this is within limits.

The choice of $C_P R_P$ of Fig. 5.6.1 must be large enough to avoid loading of trigger source and at the same time must be small enough to allow complete discharge during one time period.

Select $C_P = 82$ pf $R_P = 10 K\Omega$

$$C_P R_P = 82 \times 10^{-12} \times 10 \times 10^3 = .82 \ \mu s.$$

As one time period is .. this time constant is small enough to ensure complete discharge during one time period.

Final design figures as shown in Fig. 5.6.1 are:

$R_C = 820\,\Omega$, $R_K = 4.7K\,\Omega$, $R_A = 4.7K\,\Omega$, $R_T = 4.7K\,\Omega$,
$R_F = 10K\,\Omega$, $R_B = 75K\,\Omega$, $C_P = 82$ pf, $C_K = 56$ pf, $C_T = 56$ pf.

5.7 MONOSTABLE MULTIVIBRATOR

The monostable circuit, as shown in Fig. 5.7.1, has one stable state and one quasi stable state. It must be triggered into the quasi stable state and has a pulse output equal in width to the relaxation time of the circuit. Current through the resistor R_D normally holds Q_2 ON. C_D is charged to V_s through the output circuit of Q_1. When the circuit is triggered by turning Q_1 ON, C_D discharges through Q_1 and Q_2 until Q_2 turns OFF. Q_2 is then reverse biased by a voltage V_s stored on C_D. C_D now starts to charge to V_{cc} through R_D. When the voltage at the base of Q_2 is such that it is slightly forward biased, collector current will flow. The resulting drop V_{ces2} is coupled to Q_1 by C_K which causes Q_1 to turn OFF.

Before the next trigger pulse arrives the capacitor must be charged to V_s. But V_s must be limited to BV_{ebo} of Q_2. This is ensured by R_S. Taking a Thevenin's equivalent at A, circuit in Fig. 5.7.1 reduces to one shown in Fig. 5.7.2. Writing the nodal equation at B in Fig. 5.7.4

$$I^*_{L1} = (\underline{V}_{cc} - \underline{V}_1)/R^*_C - I^*_{c12} - (\underline{V}_1 - V^*_{bes2})/\underline{R}_K$$

$$I^*_{L_1} = ((1-n_P)V_{cc}-V_1)/(1+n_R)R_C - (V_1-V^*_{bes})/(1-n_R)R_K - I^*_{c12} \quad 5.7.3$$

Writing the nodal equation in Fig. 5.7.3 at C

$$I_{b11} = I_{k0} - I_{s0} = 0$$

$$\frac{V^*_{ces2} + V_{obl}}{(1-n_P)\,R_K} - \frac{(1+n_P)\,V_{bb} + V_{obl}}{(1+n_R)\,R_B} + I^*_{b11} = 0 \quad 5.7.4$$

Writing the nodal equation at D in Fig. 5.7.4

$$I_{k1} - I_{b1} - I_{s1} = 0$$

$$\frac{V_1 - V^*_{bes1}}{(1+n_R)\,R_K} - \frac{(1-n_P)\,V_{bb} + V_{bes1}}{(1-n_R)\,R_B} - I_{b1} = 0 \quad 5.7.5$$

$T = C\,R \quad \ln (V_F - V_1)/(V_F - V_c(t))$ where V_F = final capacitor voltage, V_1 = initial capacitor voltage, $V_c(t)$ = capacitor voltage at time t.

$$\underline{T}_D = \underline{C}_D\underline{R}_D \ln \left(\frac{V^*_{cc} + I^*_{b12}\,\underline{R}_D - V^*_{ces1} - V^*_{bes2} - \underline{V}_s}{V^*_{cc} - V_{tf2} + I^*_{b12}\,\underline{R}_D}\right) \quad 5.7.6$$

$$= \underline{R}_D\,\underline{C}_D \ln (\underline{X}_u) \quad \text{where}$$

$$\underline{X}_u = \frac{V^*_{cc} + I^*_{b12}\,\underline{R}_D + \underline{V}_s - V^*_{ces1} - V^*_{bes2}}{V^*_{cc} - \underline{V}_{tf2} + I^*_{b12}\,\underline{R}_D} \quad 5.7.7$$

Conditions must be in stable state before next input pulse arrives.

$$T_R^* = 1/f_1^* - T_D^*$$

where f_1^* = maximum input frequency

T_R^* = maximum recovery time

$$T_D^* = R_D^* C_D^* \ln \left(\frac{V_{cc} + V_s^* - V_{cesl} - V_{bes2}^*}{V_{cc} - V_{bes2}^*} \right) = R_D^* C_D^* \ln X_u^* \qquad 5.7.8$$

where $$X_u^* = \frac{V_{cc} + V_s^* - V_{cesl} - V_{bes2}^*}{V_{cc} - V_{bes2}^*} \qquad 5.7.9$$

The maximum recovery time equation is $T_R^* = \eta R_T^* C_D^*$

η must be chosen to allow complete recovery and for a circuit without clamp η must be at least 4

$$C_D^* = \frac{T_R^*}{R_T^*} = \frac{1/f_1^* - T_D^*}{R_T^*} = \frac{1/f_1^* - R_D^* C_D^* \ln X_u^*}{R_T^*}$$

Hence $$C_D^* = \frac{1/f_1^*}{\eta R_T^* + R_D^* \ln X_u^*} \qquad 5.7.10$$

The collector current flowing through Q_1 is given by

$$I_{c1}^* = (V_s^* / R_T) + (V_{cc}^* + V_s^*)/R_D = I_{b1} \beta_{F1}^*$$

$$R_T = \frac{V_s^*}{\beta_{F1}^* I_{b1} - (V_{cc}^* + V_s^*)/R_D} \qquad 5.7.11$$

The resistor R_D should be as high as possible within limits of permitting Q_2 to saturate during stable state.

$$R_D^* = (\beta_{F2}^* / I_{c2}^*)(V_{-cc} - V_{bes2})$$

$$= \beta_{F2}^* R_{-02}(V_{cc} - V_{bes2})/V_{-cc} \qquad 5.7.12$$

Synthesis equations:

$$\eta = (T_R^* R_D^* \ln X_u^*) / T_D^* R_T$$

$$I_{c1} = V_s^*/R_T + (V_{cc}^* + V_s^*)/R_D$$

$$= \frac{V_s^* \eta T_D^*}{T_R^* R_D^* \ln X_u^*} + \frac{V_{cc}^* + V_s^*}{R_D}$$

using tolerance factors n_{R_S} and n_{R_D}

$$I_{c1} = (V_s^* T_D^* n_{R_S})/(T_R^* R_D^* \ln X_u^*) + (V_{cc}^* + V_s^*) n_{R_D}/R_D^*$$

substituting for R_D^*

$$I_{c1} = \frac{I_{c2}^*}{\beta_{F2}^*}\left[\frac{V_s^*}{V_{cc}^*}\left\{\frac{T_D^* n_{R_S}}{T_R^* \ln X_u^*} + n_{R_D}\right\} + n_{R_D}\right] \qquad 5.7.13$$

$$\lambda \triangleq \frac{V_s^*}{V_{cc}^*}\left[\frac{T_D^* n_{R_S}}{T_R^* X_u^*} + n_{R_D}\right] + n_{R_D} \qquad 5.7.14$$

$I_k = 2I_{c1}^* / \beta_{F1}^*$ (as in flip flops).

$$I_{c2} = \gamma (I_1 + 2I_{c2}/\beta_{F1} \beta_{F2}) + I_0^*$$

$$= (\gamma I_1 + I_0^*) / (1 - (2\gamma\lambda/\beta_{F1}^* \beta_{F2}^*)) \qquad 5.7.15$$

Knowing I_{c1}^* and I_{c2}^* transistors can be chosen.

$$T_D^* = R_D^* C_D^* \ln X_u^*$$

$$\underline{T}_D = \underline{R}_D \underline{C}_D \ln \underline{X}_u$$

Hence $$T_D^* = (N_R N_C \ln X_u^*) / \ln \underline{X}_u$$

The Thevenin's voltage and resistance at the collector terminal of transistor 1 is given by

$$V_s = V_{cc} R_S / (R_S + R_P) \qquad 5.7.17$$

$$R_T = R_S R_P / (R_S + R_P) \qquad 5.7.18$$

$$V_s^*/\underline{V}_s = n_P N_R^2$$

Specifications:

Required timing $\underline{T}_D$ = .34 us f_1 = 1 Mc/s

	Available pulse input level				Required pulse output level			
	Volt		Current		Volt		Current	
	min	max	min	max	min	max	min	max
V_0	0	-.3V	0	.0025mA	0	-.3V	0	.0025mA
V_1	-3V	-6.3V	.5mA	.5 mA	-3V	-6.3V	0	3.0 mA

Design procedure:

γ = 2.58 (from flip flop design).

$$I_{c2} = \gamma I_1^* + I_0^* = 2.58 \times 3 = 7.75 \text{ mA}$$

$$\underline{I}_{b2} = I_{c2}/\beta_F^* = 7.75/20 = .386 \text{ mA}$$

$$Q_c = \underline{I}_b T_D = .386 \times 340 \times 10^{-3} \times 10^{-6} = 131 \text{ pC}$$

B V_{ebo} for 2N995 is 4V.

Hence $V_s = .9 \times 4 = 3.6V$.

From equation 5.7.9 $X_u^* = (V_{cc} + V_s^* - V_{ces} - V_{bes})/V_{cc} - V_{bes}^*$

$= (5.7 + 3.6 - .2 - .7)/5.7 - .7 = 1.6$

From equation 5.7.7 $V_s = V_s^*/(n_P N_R^2 = 3.6/(1.105 \times 1.105^2) = 2.68V$

$$X_u = \frac{V_{cc} + V_s - V_{ces1}^* - V_{bes2}^*}{V_{cc}^* - V_{TF2}} = \frac{6.3 + 2.68 - .2 - .7}{6.3 - 0.1} = 1.32$$

$X_u^* = 1.66$, $\ln X_u^* = .51$

$X_u = 1.32$, $\ln 1.32 = .278$

$T_{Do}^*/T_o = N_{R_D} N_C \ln X_u^* / \ln X_u = (1.105 \times 1.105 \times .51)/.278 = 2.24$

$T_D^* = T_D \times 2.24 = 340 \times 2.24 = 760$ ns

Substituting in equation 5.6.14

$$\lambda = \frac{3.6 \times 7.6}{6.3 \times 2.4} \left(\frac{4 \times 1.105}{.51} + 1.105 \right) + 1.105 = 18.905$$

$I_{c1}^* = I_{c2}^* / \beta_{F1}^* = 18.905 \times 7.75 / 20 = 7.35$ mA

$I_{c2} = (I_1^* \gamma + I_0^*) / (1 - 2\gamma / (\beta_{F1}^* \beta_{F2}^*))$

$= 3 \times 2.56 / (1 - 2 \times 2.58 \times 18.905/(20 \times 20)) = 10.2$mA

$I_{c1} = 18.905 \times 10.2 / 20 = 9.8$ mA

R_C, R_K and R_B are now calculated from equations 5.7.3, 5.7.4 and 5.7.5.

$$\frac{V_{-cc} - V_{-1}}{(1+n_R)\,R_{C2}} - \frac{V_{-1}}{(1-n_R)\,R_K} = I_1 + I_{cl2}$$

$$\frac{5.7 - 3.0}{(1+.05)\,R_{C2}} - \frac{3.0}{.95\,R_K} = 3 + .00256$$

$$1/R_{C2} = (3.00256 + 3.16/R_K)/2.57 \qquad 5.7.19$$

From equation 5.6.4, we have

$$\frac{V_{-bb} - V_{-obl}}{(1+n_R)\,R_B} - \frac{V^*_{obl} + V^*_{ces2}}{(1-n_R)\,R_K} = I_{bli}$$

$$(5.7 - .1)/1.05\,R_B - (.1 + .2)/.95\,R_K = .00256$$

$$1/R_B\ (.00256 + .316/R_K)\ /\ 5.35 \qquad 5.7.20$$

From equation 5.7.5, we have

$$\frac{V_{-bb} + V^*_{besl}}{(1 + n_R)\,R_B} - \frac{V^*_{cc}}{\beta^*_{F1}\,\beta^*_{F2}(1-n_R)R_{C2}} + \frac{V_1 - V_{besl}}{(1+n_R)\,R_K} = 0$$

$$- \frac{5.7 + .6}{1.05\,R_B} - \frac{18.905 \times 6.3}{20x20x.95\,R_{C2}} + \frac{3 - .6}{1.05\,R_K}$$

R_B and R_{C2} are substituted from equations 5.7.19 and 5.7.20.

$$- \frac{6}{5.35}\left(.00256 + \frac{.316}{R_K}\right) - \frac{.314}{2.57}\left(3.00256 + \frac{3.16}{R_K}\right) + \frac{2.29}{R_K}, = 0$$

Hence $R_K = 1.548/.37008 = 4.2K\Omega$.

$R_K = 4.7K\Omega$ is selected.

From equation 5.7.19

$1/R_{C2} = (3.00256 + 3.16/4.7)/2.57$. Hence $R_{C2} = 720\,\Omega$

$R_{C2} = 820\,\Omega$ is selected.

From equation 5.7.20

$1/R_B = (.00256 + .316/4.7) / 5.33$. Hence $R_B = 76K\,\Omega$.

$R_B = 75K\,\Omega$ is selected.

Now we have to check conditions of reverse bias with these figures

$$V_{obl} = \frac{V_{-bb} R_K - V^*_{ces2} R^*_B - I_{bl} R_{-K} R^*_B}{R_{-K} + R^*_B}$$

$$= \frac{5.7 \times 4.7 \times .95 - .2 \times 75 \times 1.05 - .00256 \times .95 \times 1.05 \times 4.7 \times 75}{4.7 \times .95 \times 75 \times 1.05}$$

$$= .114 \text{ volts.}$$

This is sufficient to reverse bias transistor and does not exceed V_{ebo}.

From equation 5.7.12

$$R_D = \frac{(V_{-cc} - V^*_{bes2}) \beta^*_{F1} R_{-C2}}{V_{-cc}(1+n_R)(1+ I^*_0 R_{C2}/V_{cc})} = \frac{(5.7 - .6) \times 20 \times .95 \times 820}{5.7}$$

$R_D = 13.3K\,\Omega$. Hence select $R_D = 15K\,\Omega$.

Hence $R^*_D = 15.8\,\Omega$, $R_{-D} = 14.8K\,\Omega$.

$$C_D = (T_D/R_{-D})/\ln((V^*_{cc} + I_{bl} R_D + V_{-s} - V_{ces1} - V_{bes2})/(V^*_{cc} - V_{TF} + I_{bl} R_D))$$

$$= 340 \times 10^{-9} / 14.2 \times 10^{-3} \ln 8.32/6.392 = 82 \text{ pf}$$

$$I_{b1} = \frac{V_{-1} - V^*_{besl}}{R^*_K} - \frac{V_{bb} + V^*_{besl}}{R_S}$$

$$= \frac{3 - .6}{1.105 \times 4.7} - \frac{6.3 + .6}{.95 \times .75} = .398 \text{ mA}$$

$$R_T = \frac{V^*_s}{\beta_{F1} I_{b1} - \frac{V^*_{cc} + V^*_s}{R_D}} = \frac{3.6}{20 \times .389 - \frac{6.3 + 3.6}{14.2}} = 510\,\Omega$$

R_T = 750 Ω is selected.

$$V^*_s = \frac{V^*_{cc}\ (1+n_R)\ R_S}{(1+n_R)\ R_S + (1-n_R) R_P} = \frac{6.3 \times 1.05 \times R_S}{1.05\ R_S + .95\ R_P} = 3.6\text{V}$$

$$R_S = .95 \times 3.6 \ / \ (1.05 \times 2.7) = 1.22\ R_P$$

$$R_T = \frac{(1-n_R)\ R_P\ (1-n_R)\ R_S}{(1-n_R)\ R_P + (1-n_R) R_S} = \frac{R_P \times .95\ R_S}{R_P + R_S} = 510\,\Omega$$

$$R_P = 2.2 \times 510 \ / \ .95 \times 1.22 = 985\,\Omega$$

R_P = 1KΩ is selected.

R_S = 1.22 x 1 = 1.2KΩ . Hence R_S = 1.2KΩ is selected.

In Fig. 5.7.1, the designed values are:

R_C = 820 Ω , R_B = 75KΩ , R_P = 1KΩ , R_S = 1.2KΩ, C_K =56 pf, R_K = 4.7KΩ , R_i = 10KΩ , C_i = 470 pf C_D and R_D are fixed from required time period.

5.8 LAMP DRIVERS

• The lamp drivers are used to give visual indication of the states of various registers in the computer. Lamp drivers should be such that they do not affect the fan-out capability of a circuit to which they are connected. A high input impedance (so as to produce negligible loading on source) is obtained by connecting the lamp drivers in the Darlington configuration.

If I_L = current required to light lamp
R_L = lamp resistance

In Fig. 5.8.1, $I_{c_1} = I_L = (V_{cc} - V_{ces2})/(R^*_{C2} + R^*_L)$

$$R^*_{C2} = (V_{cc} - V_{ces2})/I_L - R^*_L \qquad 5.8.1$$

$$I_{b_1} = I_{c_1} / \beta_{F1}$$

$$I_{c_2} \simeq I_{e_2} \simeq I_{b_1} = I_{c_1} / \beta_{F1}$$

$$I_{b_2} = I_{c_2} / \beta_{F2} = I_{c_1} / \beta_{F1} \beta_{F2}$$

$$I^*_{b_2} = \frac{V_1 - V_{bes2}}{R_{B1}} = \frac{I_{c_1}}{\beta^*_{F1} \beta^*_{F2}} = \frac{I_L}{\beta^*_{F1} \beta^*_{F2}}$$

$$R_{B1} \qquad \frac{(V_1 - V_{bes2}) \beta^*_{F1} \beta^*_{F2}}{I_L} \qquad 5.8.2$$

Design Procedure:

Specifications:

	Input volts min	Input volts max	Input current min	Input current max	Output
V_0	0	-.3V	0	.0025mA	lamp OFF
V_1	-3V	-6.3V	20uA	30uA	lamp ON

Lamp specifications:- 135 mA, 6V, 250 mW, 20

From equation 5.8.1

$$R^{*}_{C2} = (V_{cc} - V^{*}_{ces})/I_L - R^{*}_{C} = (5.7 - .1)/135 \times 10^{-3} - 20 = 15$$

$$P_D \Big|_{\text{resistance}} = .135 \times .135 \times 15 = .283W$$

Hence R_{C2} selected is 15 Ω, 1/2W.

$$P_D \Big|_{\text{transistor}} = 135 \times 1 = 135 \text{ mW}.$$

This is within the transistor rating.

$$I_{b_2} = I_{e_1} = I_{c_1}$$

$$I_{b_2} = I_{c_1} / \beta_{F1} = 100/20 = 5.0 \text{ mA}$$

$$I_{b_1} = 5.0/150 = 33.4 \times 10^{-3} \text{ mA}$$

$$R^{*}_{B2} = \frac{V_1 - V_{bes1}}{I_{b_1}} = \frac{2.3}{33.4 \times 10^{-6}} = 70K\Omega$$

Hence selected $R_B = 75K\Omega$

In Fig. 5.8.2 the design figures are $R_B = 75K\Omega$, $R_C = 15\Omega$, lamp 6V, 250mW, 20 Ω.

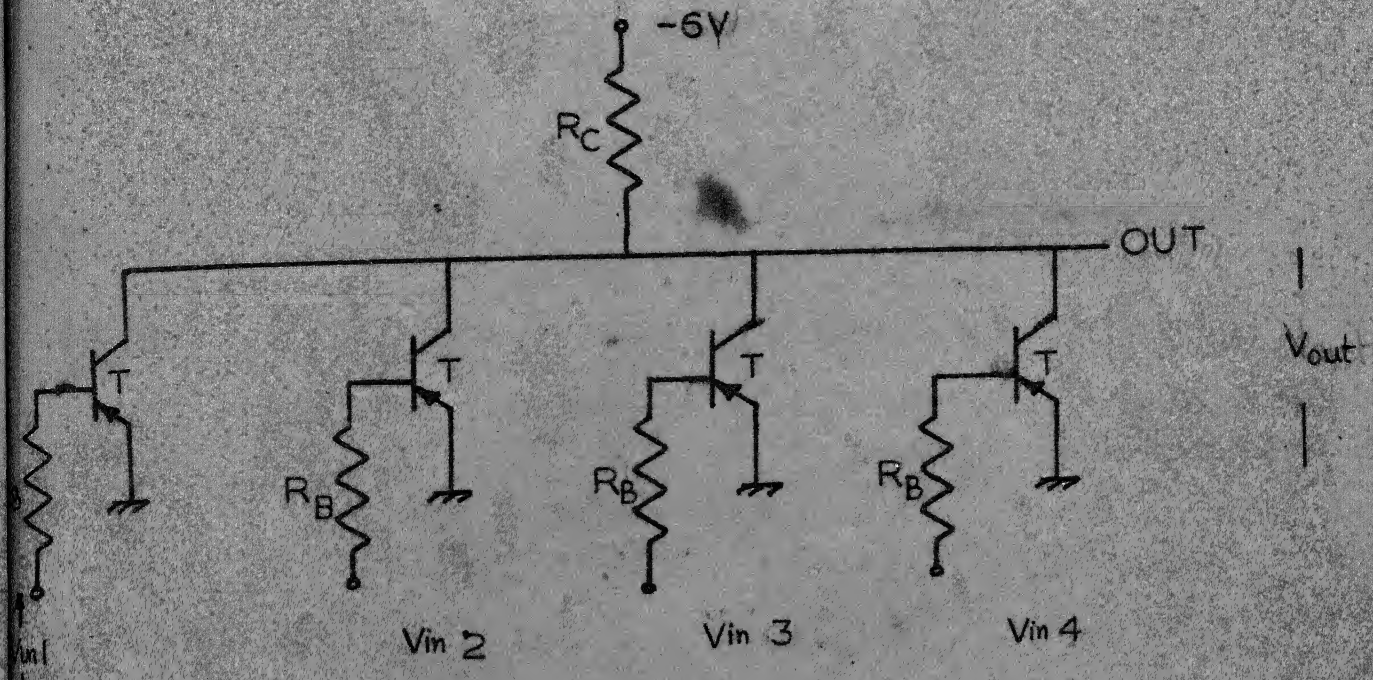


FIG_5.1.1 BASIC 4-INPUT TRL GATE

T = 2N995 R_C = 1KΩ R_B = 4.7KΩ

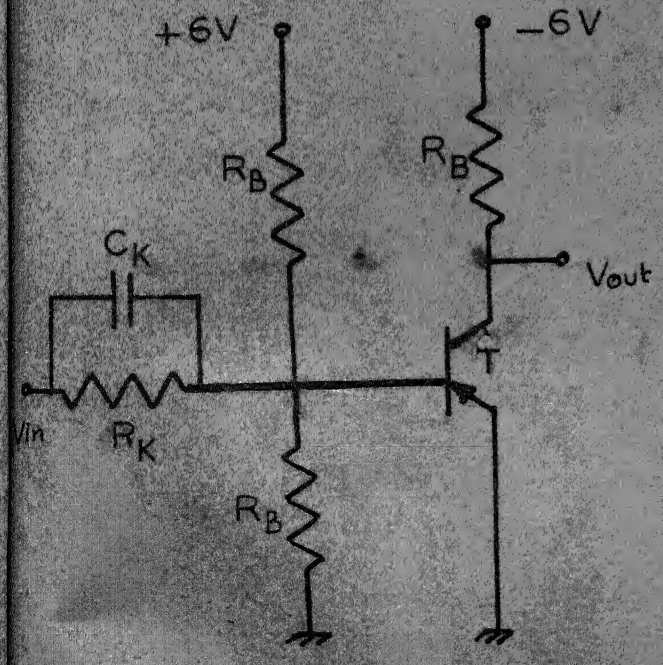


FIG.5.1.2 BASIC INVERTER CIRCUIT

R_B=75K R_K=4.7K R_C=820Ω

C_K = 56 pf.

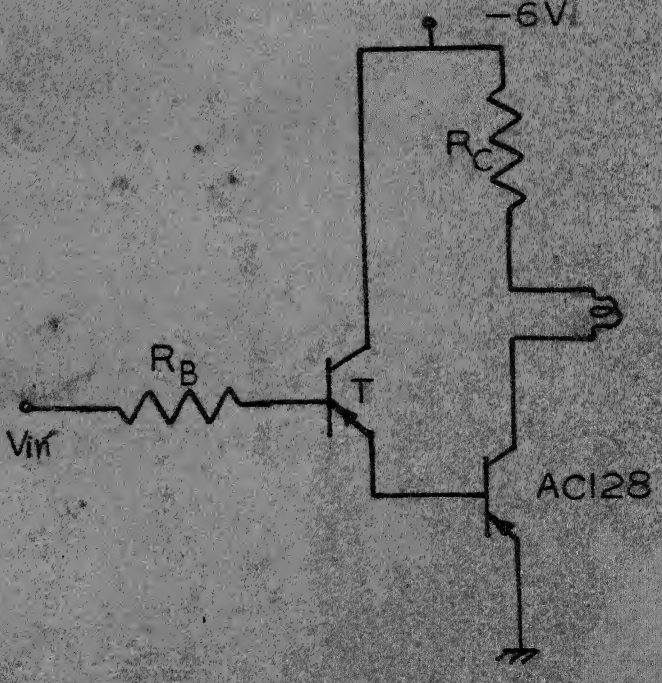


FIG._5.1.5 LAMP DRIVER CIRCUIT

R_C = 40Ω. R_B = 46KΩ.

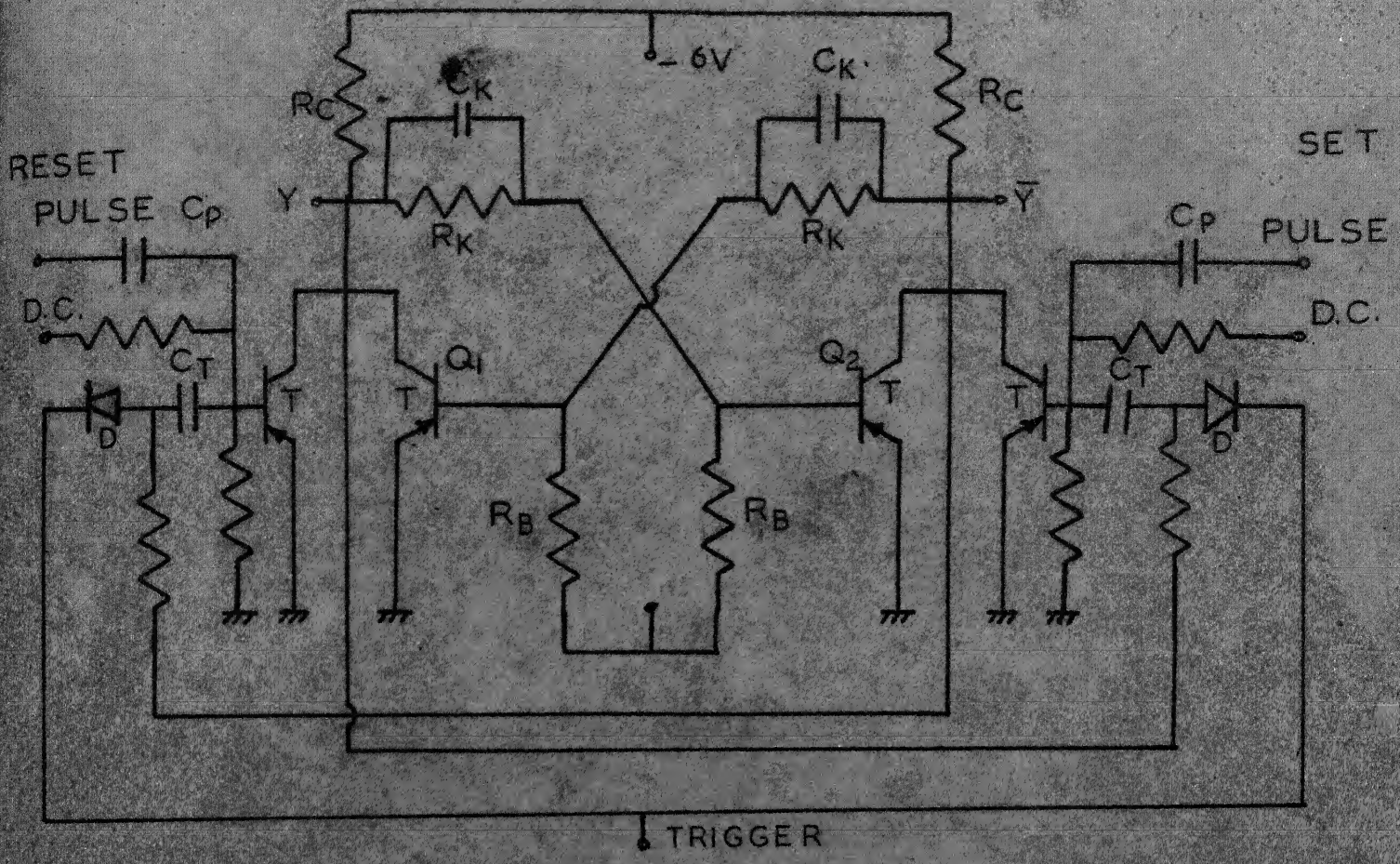


FIG-5.1.3 FLIP FLOP CIRCUIT.

R_C=820R R_K=5.7K R_B=84K R_T=4.7K R_P=10K R_A=4.7K
C_K=56p C_T=56p C_P=56p T= 2N995 D=CD21

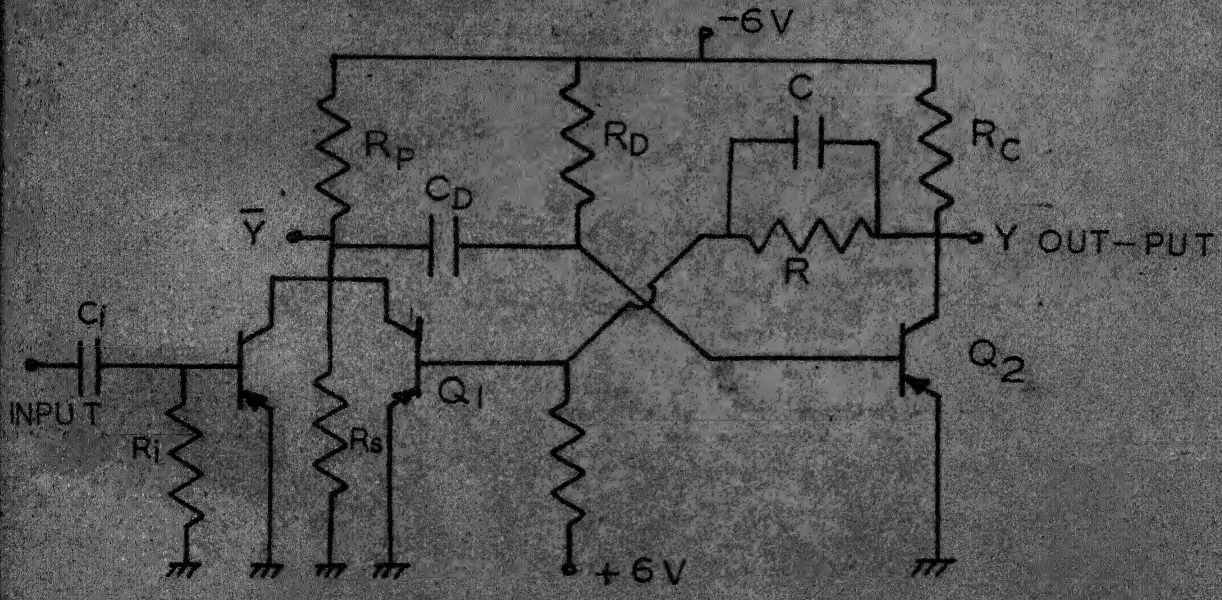


FIG 5.1.4 MONOSTABLE CIRCUIT

R_C 880Ω R_K 5.7K R_B=84K R_P=750Ω R_D=15K R_i = 10K
C_K=56p

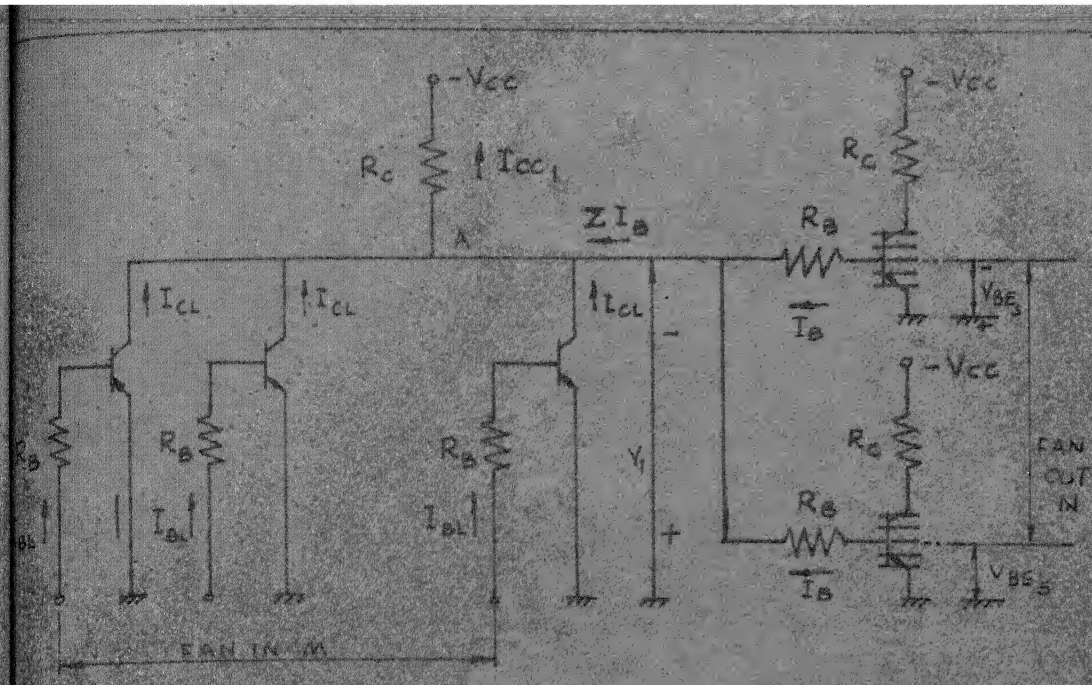


FIG 5.1
CONDITIONS WITH ALL TRANSISTORS OFF

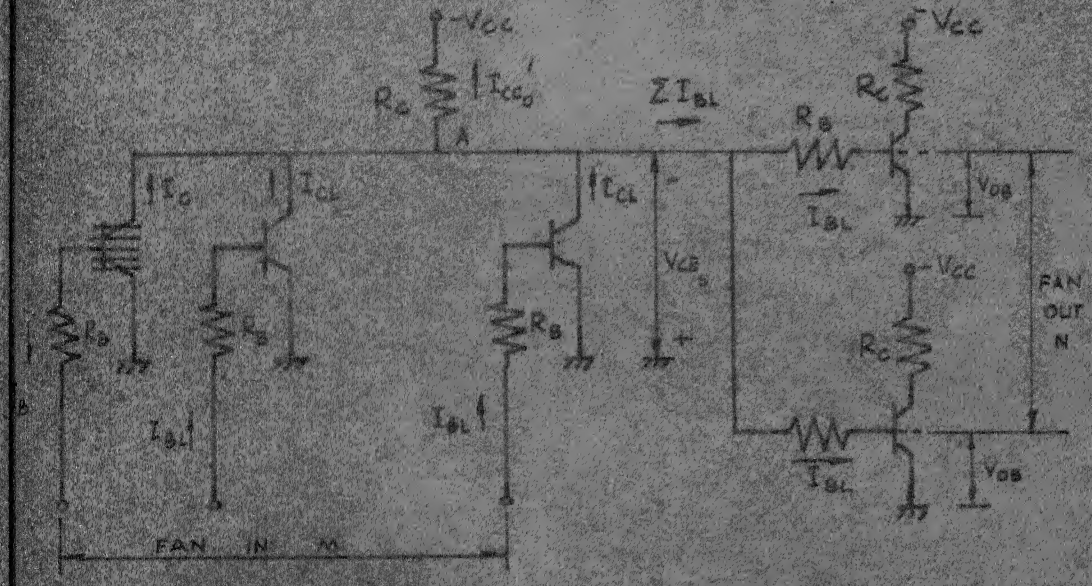


FIG 5.2
ONE TRANSISTOR CONDUCTING Φ
(N-1) TRANSISTORS CUT OFF

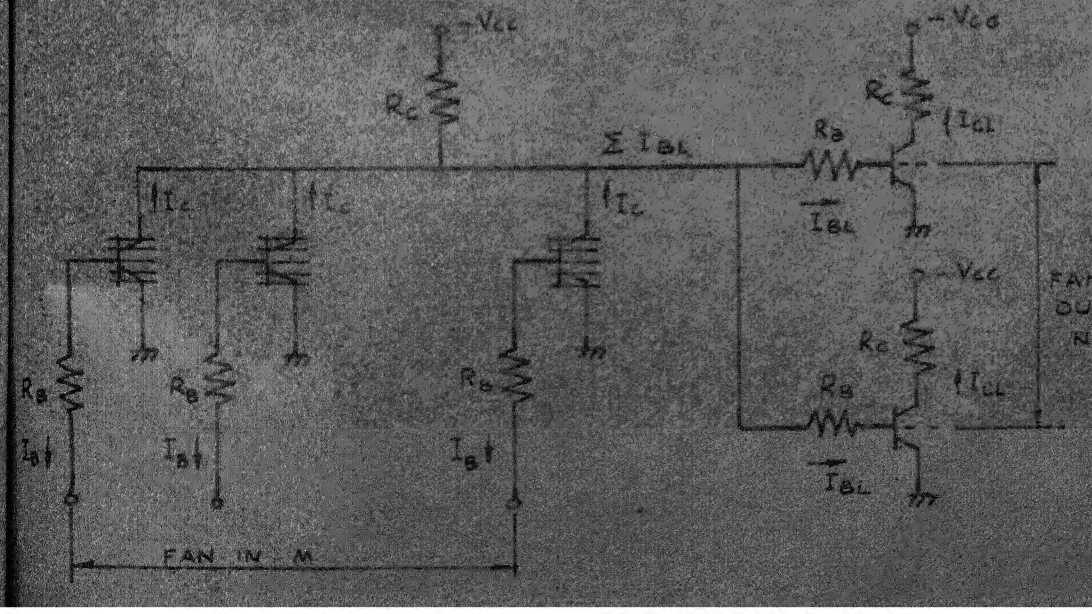


FIG 5.3
ALL TRANSISTORS CONDUCTING

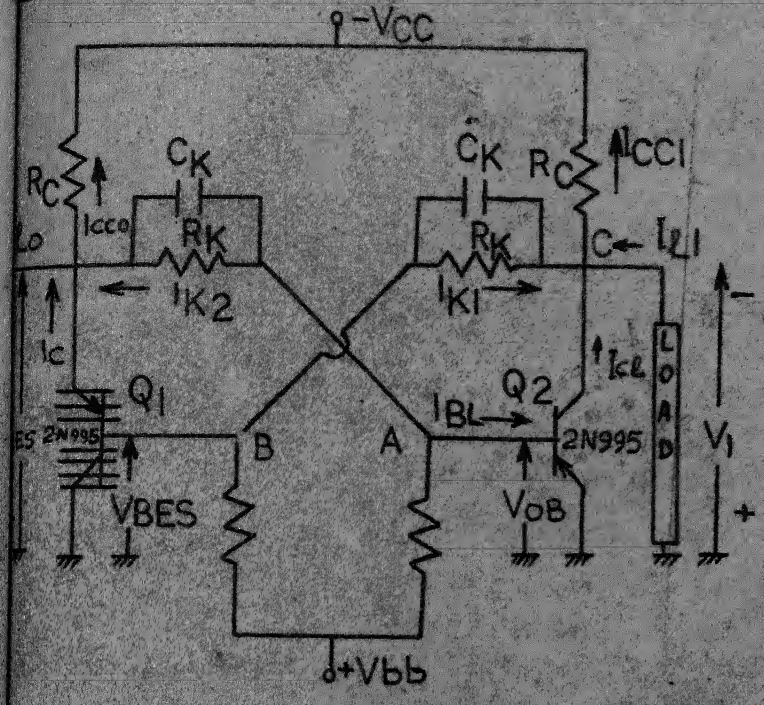


FIG.5.6.2 :- FLIP FLOP CONDITION Q_1 ON & Q_2 OFF

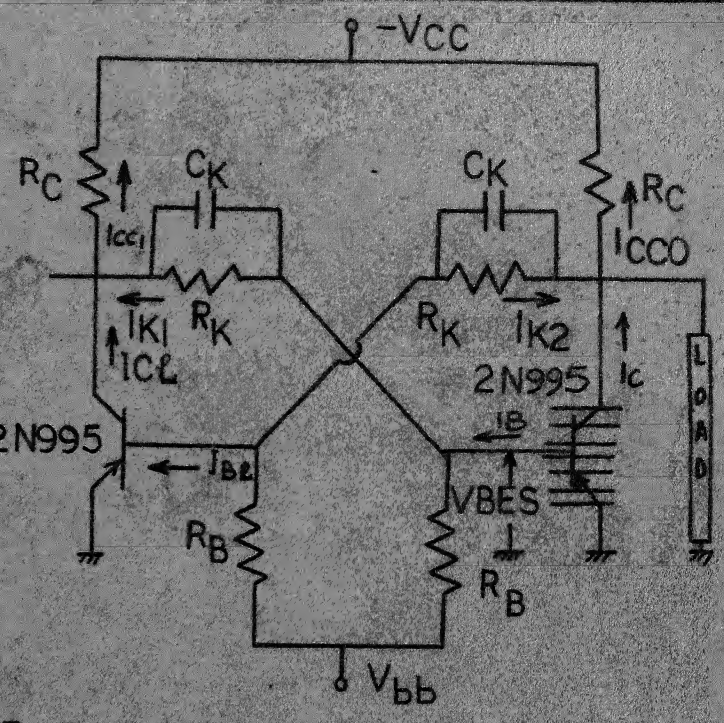


FIG.5.6.3 FLIP FLOP CONDITION Q_1 OFF & Q_2 ON

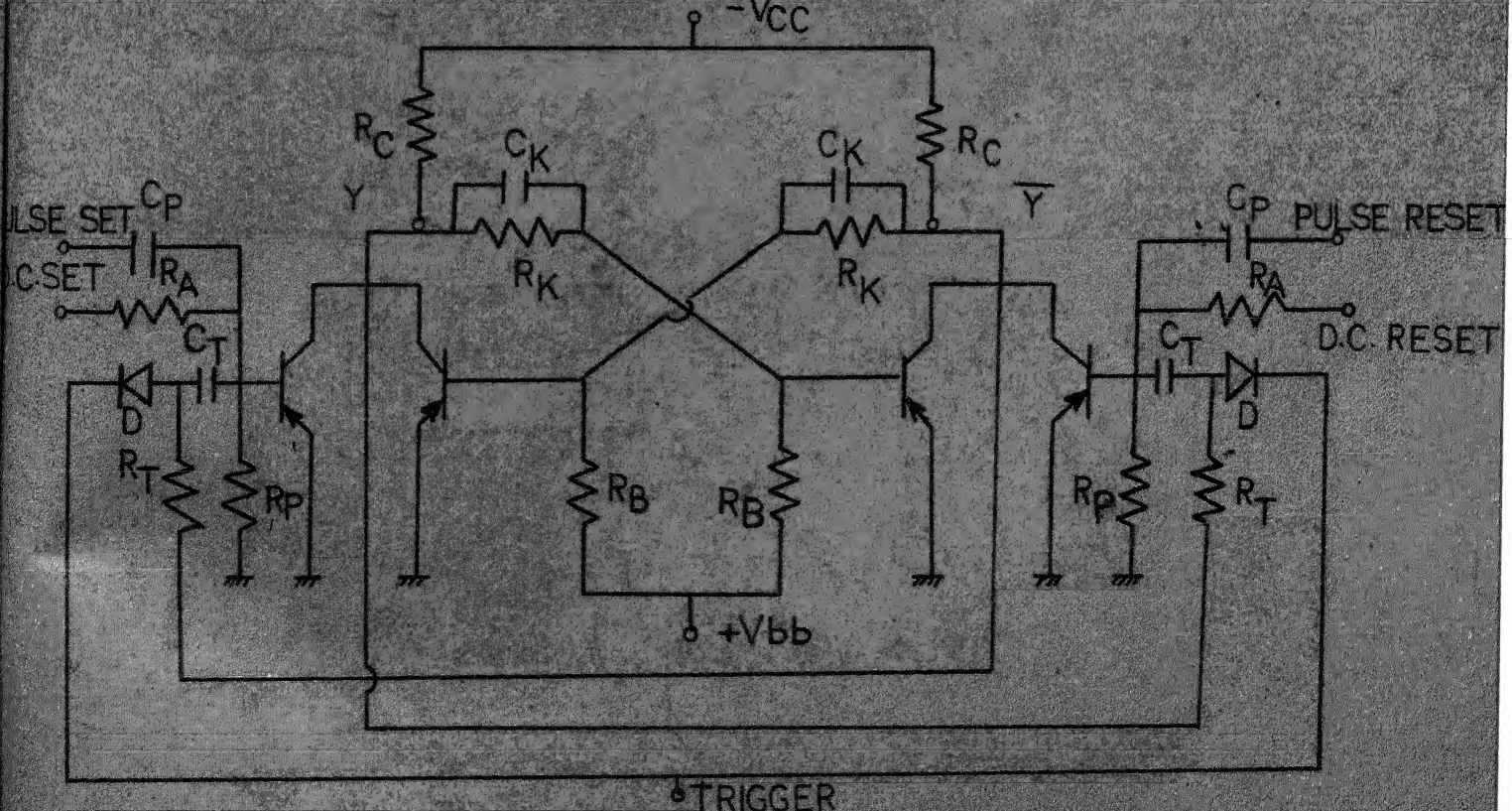
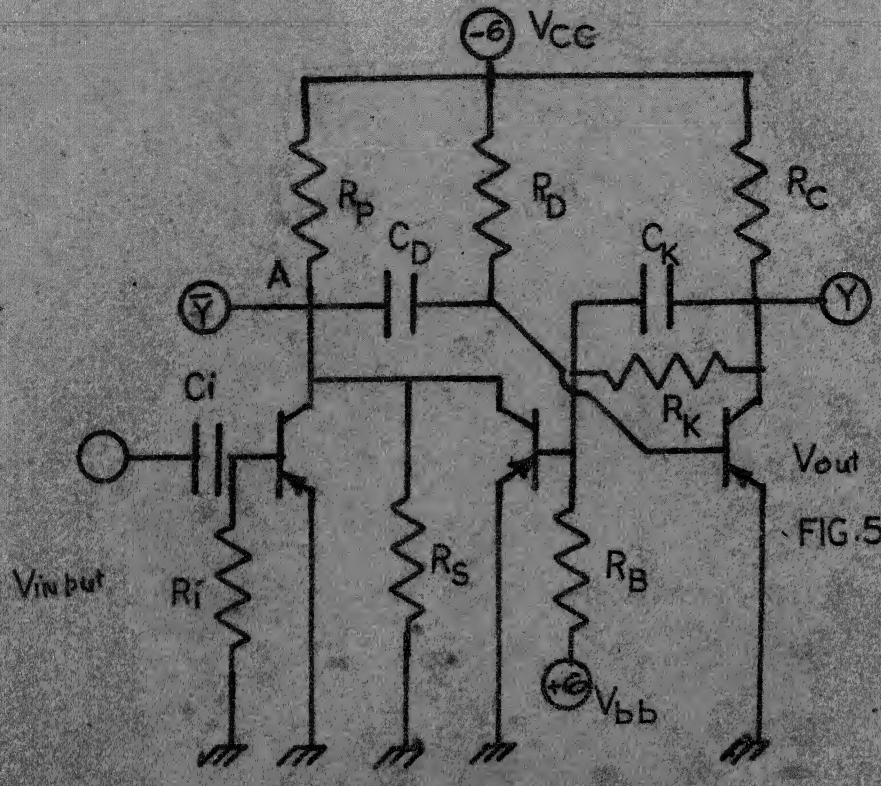


FIG.5.6.1 BASIC FLIP FLOP CONFIGURATION WITH TRIGGER AMPHFIER TRANSISTORS 2N995 DIODES CD 21 R_C = 820 Ω R_K = 4.7K Ω R_B = 15K Ω R_P = 10K Ω R_T = 4.7K Ω R_A = 4.7K Ω C_T = 56 pf C_P = 82 pf C_K = 56 pf



$R_C = 820\Omega$
$R_K = 4.7K$
$C_K = 56p$
$R_D = 15K$
$R_P = 750\Omega$
$R_S = 1K$
$R_i = 10K$
$R_B = 75K$
$C_i = 470p$

FIG.5.7.1 BASIC ONE SHOT CIRCUIT

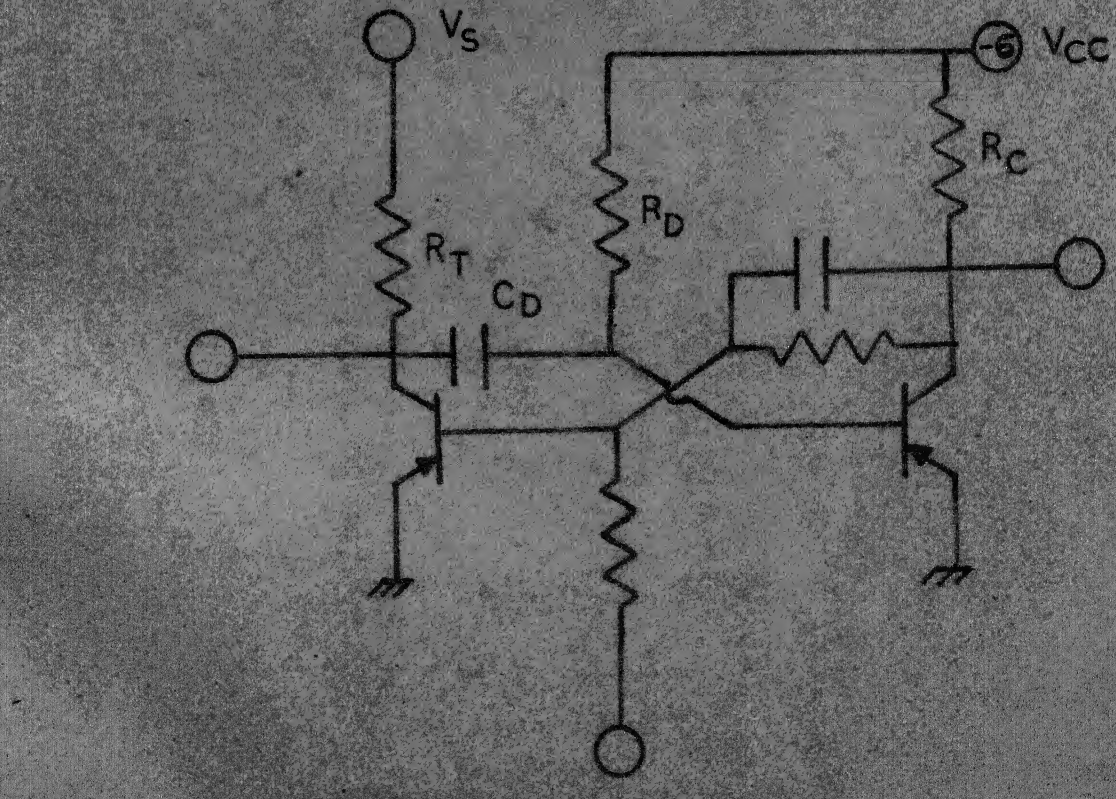


FIG.5.7.2:- ONE SHOT CIRCUIT AFTER APPLYING THEVENINS THEORAM AT A

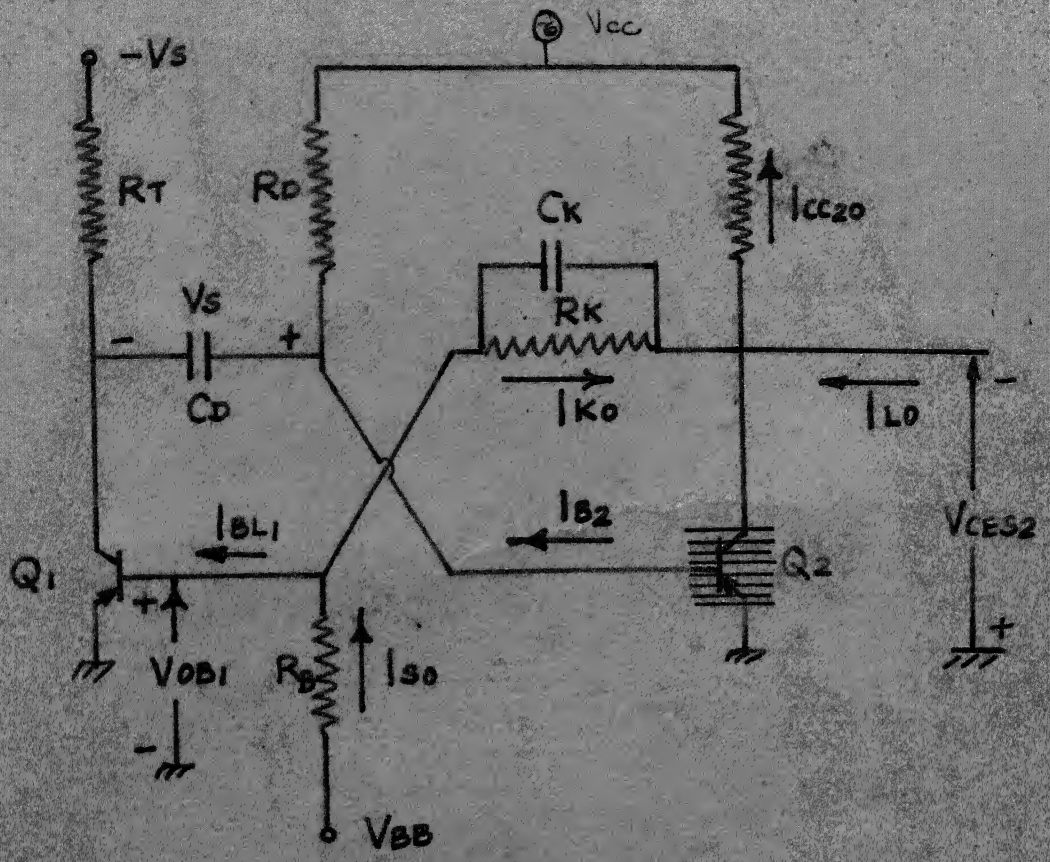


FIGURE 5.7.3 MONOSTABLE STABLE STATE

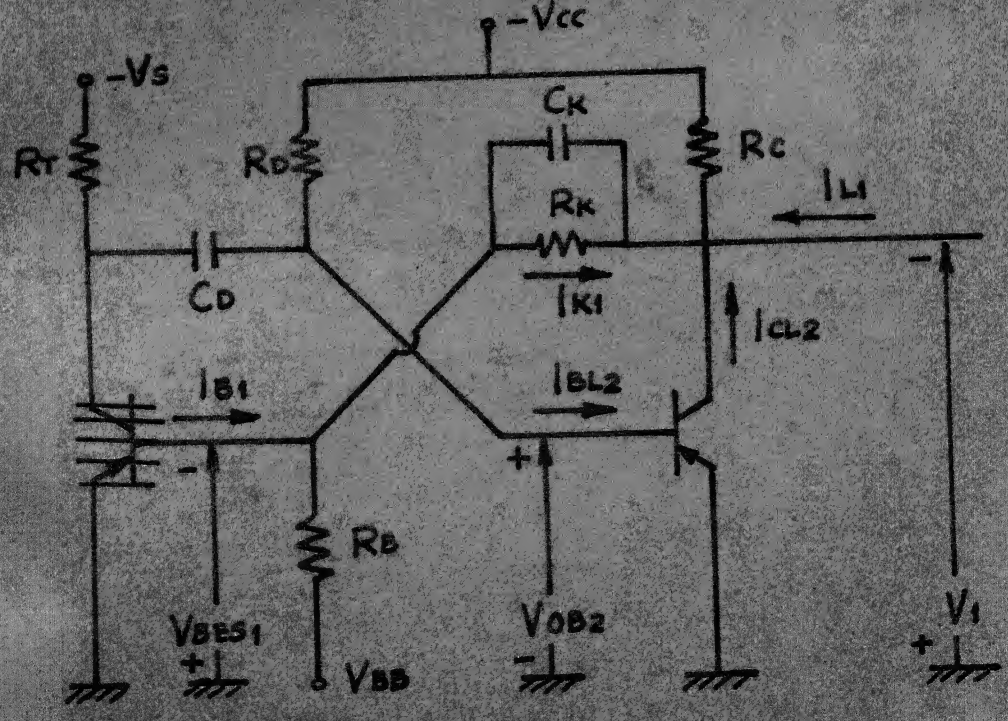


FIGURE 5.7.4. MONOSTABLE QUASISTABLE STATE

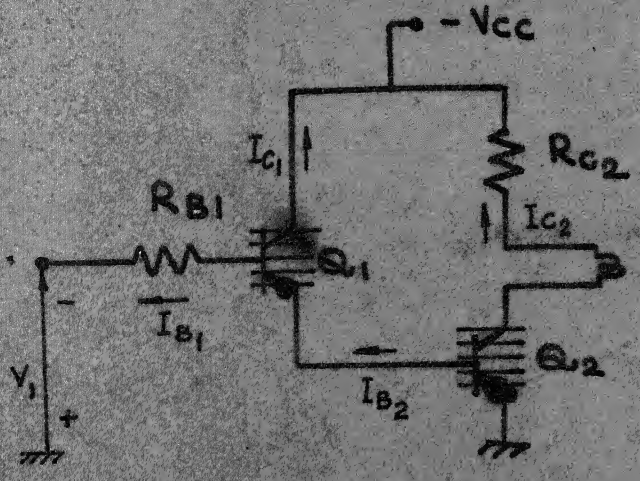


FIGURE 5·8·1 CONDITION WHEN LAMP IS LIGHTED

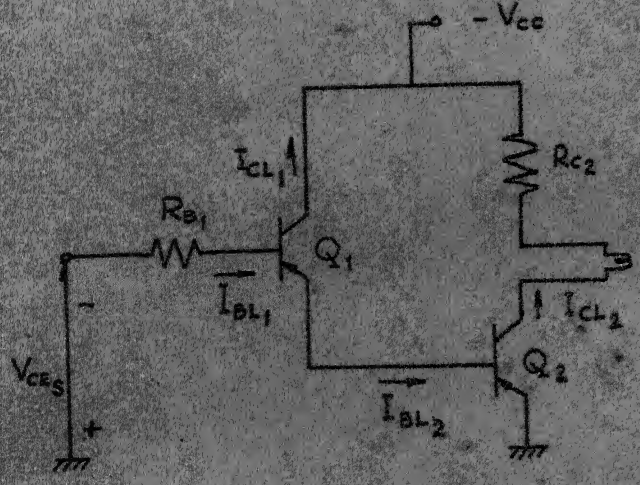


FIGURE 5·8·2 CONDITION WHEN LAMP IS OFF

DESIGNED VALUES, R_C = 15 Ω, R_B = 75 KΩ
LAMP 6V, 100mA, 250mV

CHAPTER 6

TEST PROCEDURES

Every module should be tested for functional accuracy. Only 5% of them need be subjected for transient and temperature tests. It is preferable to set up test jigs with GO, NO GO standards to indicate limits of acceptance, but at present test procedures which are basically laboratory type procedures have been outlined. Following tests have to be carried out for all cards and transient tests are described in next chapter.

6.1 TESTS FOR TRL NOR GATE

(i) 2 Input NOR Gate:

The truth table for 2 input NOR Gate is verified with a load of 1.5K Ω according to the circuit shown in Fig. 6.1.1. The '0' corresponds to -0.3V, (which is the saturated collector voltage for a 2N995 transistor) and the '1' level is -3V. Actually the '1' level can lie anywhere between -3 and -6V, and -3V is the worst case.

TRUTH TABLE 2 INPUT NOR

Vin 1	Vin 2	Vout
0	0	1
0	1	0
1	0	0
1	1	0

(ii) 4 Input NOR Gate:

The truth table for the 4 Input NOR Gate as shown in the accompanying table, is verified using the circuit of Fig. 6.1.2. As in the previous case, the '0' level is -.3V and '1' level applied is -3V.

Vin 1	Vin 2	Vin 3	Vin 4	Vout
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

6.2 TEST FOR INVERTER CARD

8 inverters of a card are connected in cascade as shown

in Fig. 6.2.1. A .5 μs negative pulse train is applied at a PRR of 500 Kc/s and the output pulse train on the output of each inverter, i.e., at terminals 7, 9, 14 and 16 are to indicate an inversion. The output on the remaining 4 inverters, i.e., at terminals 8, 6, 14,and 17 should repeat the input pulse train. The '1' level is not to fall below -3V and '0' level is not to rise above -.3V.

The delay per stage can be measured by connecting an odd number of inverters in a ring and then measuring the period of oscillation.

$$\text{Delay/stage} = \frac{\text{Period of oscillation}}{\text{No. of stages in ring oscillator (odd)}}$$

6.3 TESTS FOR FLIP FLOP

(i) The circuit is connected as shown in Fig. 6.3.1 and a .1 us, 500 Kc/s input is applied at terminal 7. The output observed at terminal 17 should be square waves at 125 Kc/s.

(ii) The circuit is now connected as shown in Fig. 6.3.2 and output Y and $\bar{Y}$ are connected to the D.C. set and reset terminals at pins 15 and 18. A .1 us , 500 Kc/s input is applied at terminal 7. The output observed on terminal 17 should be square waves at 250 Kc/s. A -3V D.C. level is now connected to D.C. set and reset terminals one by one. On application of an input pulse train at the trigger terminal the D.C. set or reset input should prevail over the pulse

(iii) The output terminals 4 and 6 are disconnected from terminal 15 & 18 and connected to 14 & 20 according to Fig. 6.3.3. The entire procedure is now repeated with positions of Flip Flop 1 and 2 interchanged and the triggering signal applied at terminal 16. The results should be identical.

The above experiments have confirmed the flip flop changes state when the triggering signal is applied at any of the input terminals provided the flip flop is at present in the complementary state. The trigger terminal of the flip flop does not remember the previous state and changes state whenever an input pulse is applied to it.

A further check to be carried out is to see that the outputs at terminals 2 & 21 are the inverted outputs of what are available at terminals 6 & 17. A 15 KΩ unbalanced load is applied at the output terminals alternatively during these tests.

6.4 TEST FOR ONE-SHOT

The four one-shots in a card are connected in cascade as shown in Fig. 6.4.1. The complementary output of one stage is used to trigger the next stage. The input of the first one-shot is triggered at a rate lower than the combined delay of all stages and the delay between the input at terminal 3 of stage 1 and the output at terminal 21 of stage 4 is measured. The output should be delayed by a period equal to the combined delay of first three stages and its pulse width should be equal to the delay of stage 4. The 1 level on full load should not fall below -3V and the '0' level should not rise above -.3V.

6.5 TEST FOR LAMP DRIVER

The lamp drivers are driven by a -3V, 500 ms, 10 c/s input and a lamp should turn ON and OFF at 10 c/s. Next, the lamp is lit by -3V D.C. at the input and the source drain required to drive the lamp is measured. This should not exceed 40 uA. This test is repeated for all five lamp drivers. Circuit diagram for the test is shown in Fig. 6.5.1.

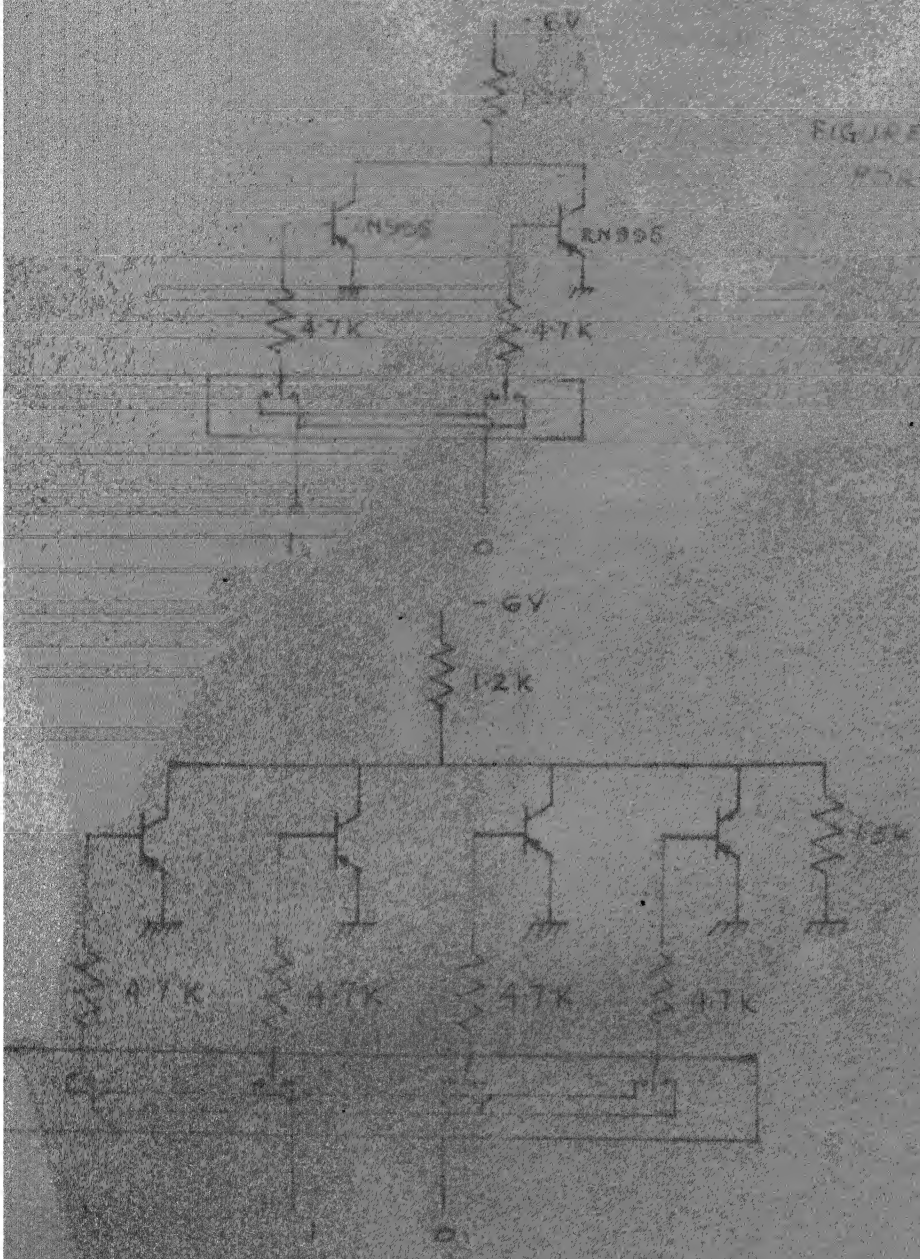


FIGURE 6.1.1 EXPERIMENT FOR 2 INPUT NOR TRUTH TABLE

6.2.1

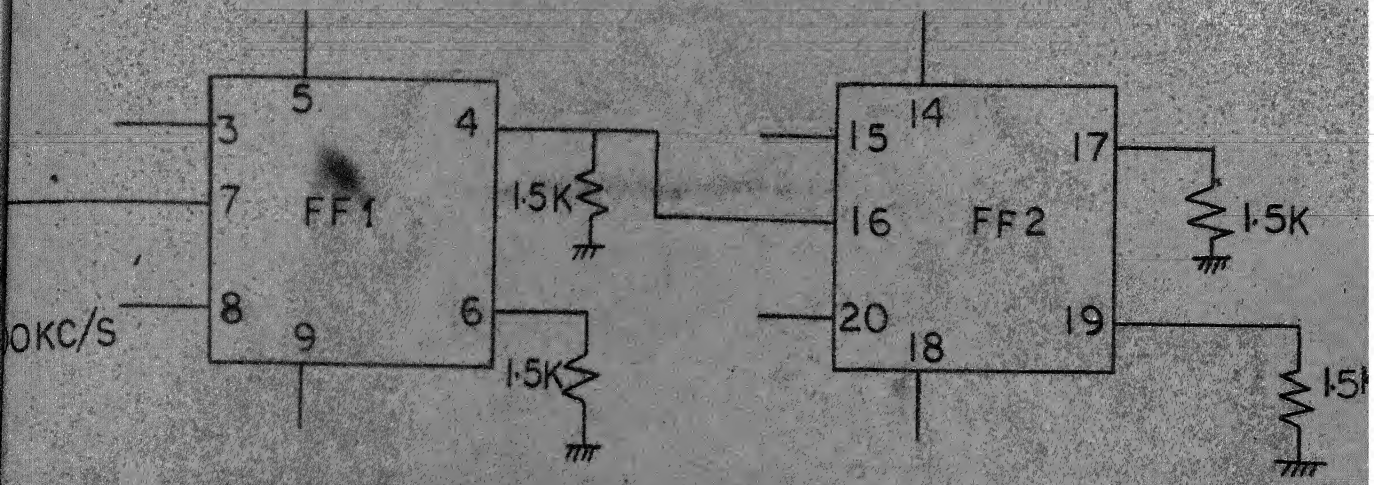


FIG 6.3.1 TEST 1 FOR FLIP FLOP

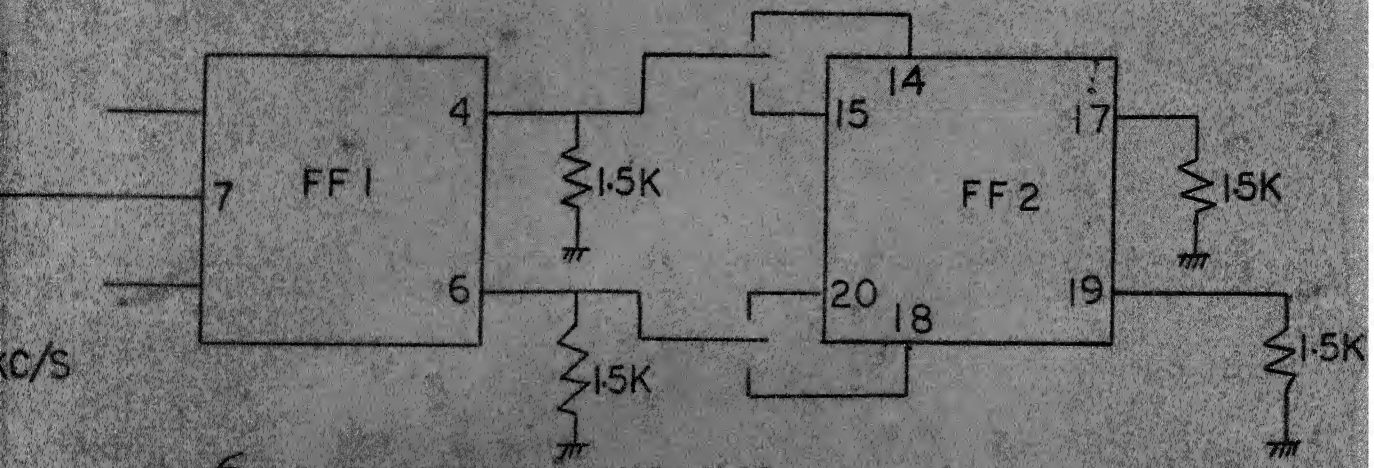


FIG 6.3.2:-TEST 2 FOR FLIP FLOP

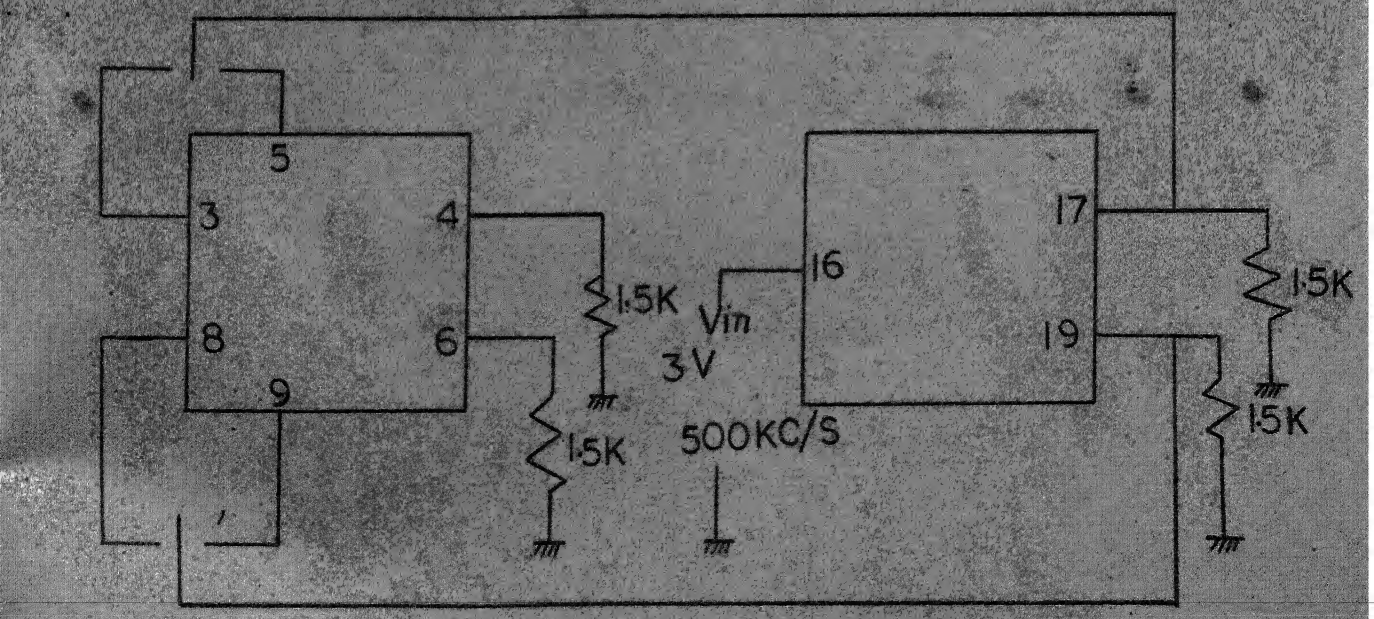


FIG 6.3.3:-TEST 3 FOR FLIP FLOP

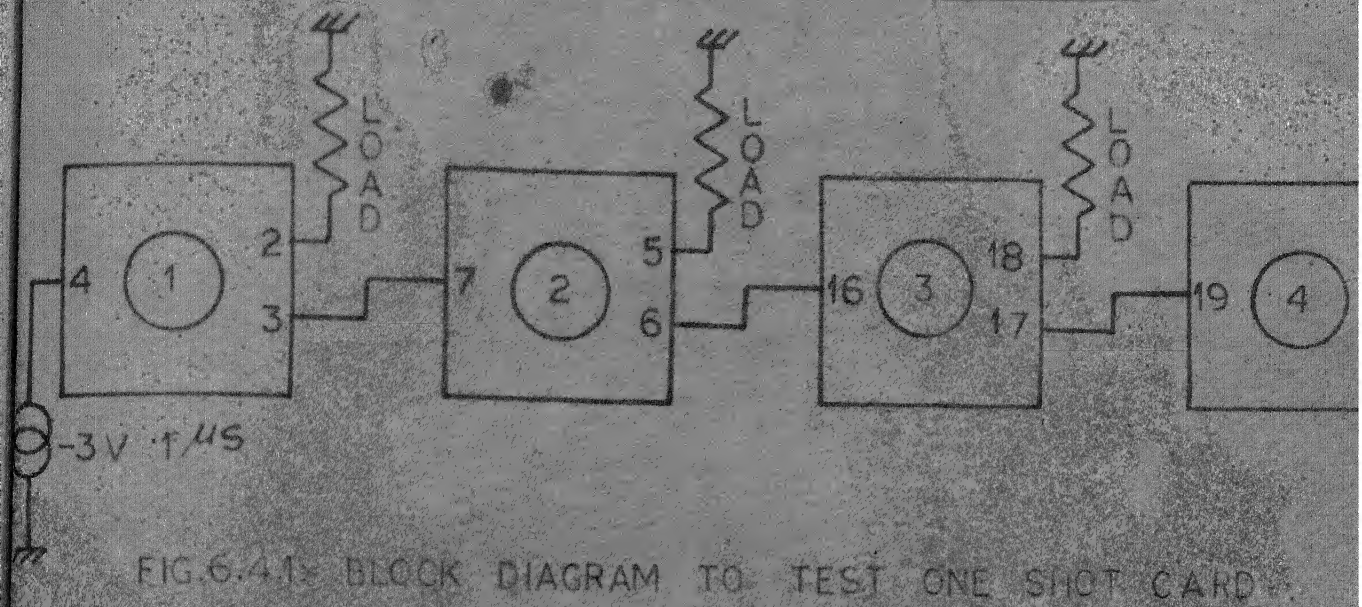


FIG.6.4.1:- BLOCK DIAGRAM TO TEST ONE SHOT CARD.

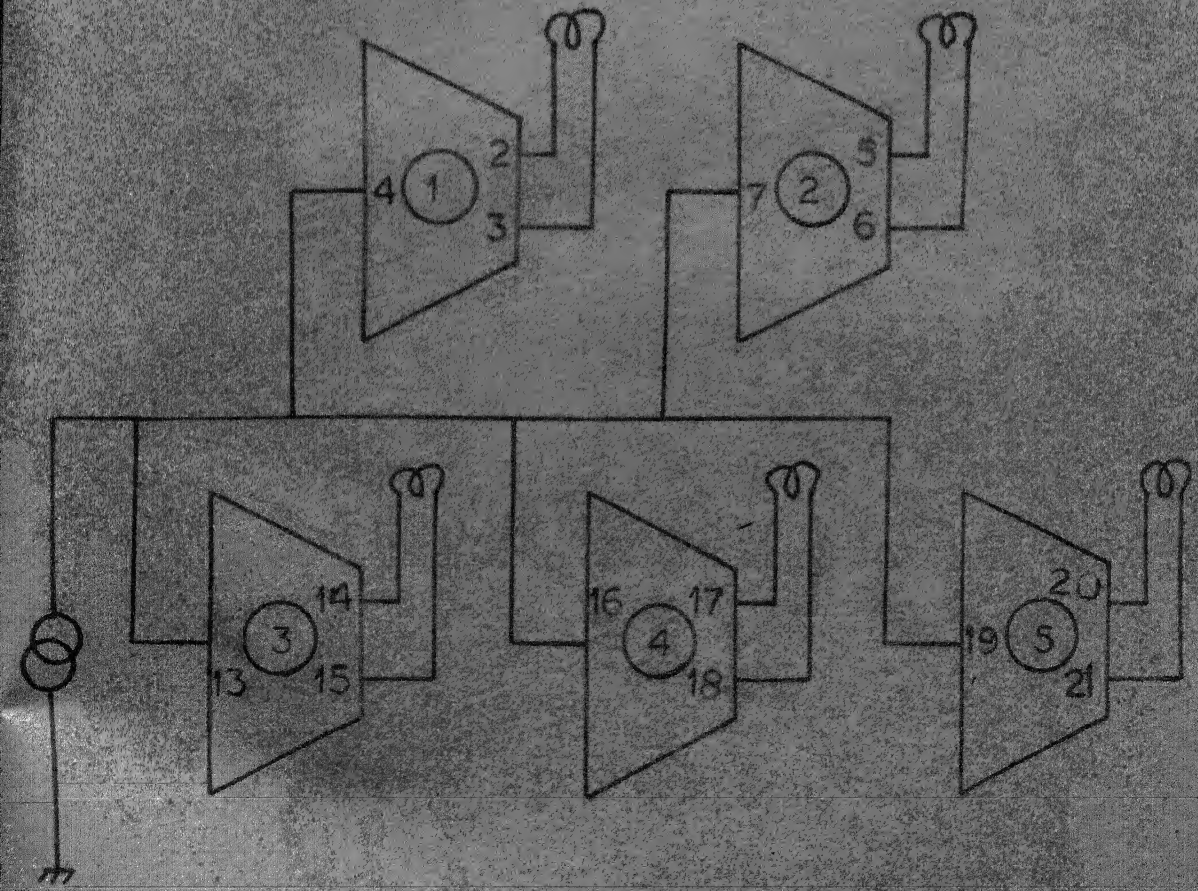


FIG.6.5.1:- CONNECTIONS TO TEST LAMP DRIVER CARD

CHAPTER 7

EXPERIMENTAL OBSERVATIONS

7.1 TRL NOR GATE

Three sets of observations were recorded to find the performances of the NOR gate card.

Set 1

This verifies the NOR function truth table with a 1.5K external load in parallel with 56 pf capacitor. Two sets of readings are recorded - one for the 2 input case and the other for the 4 input case according to the circuit diagrams shown in Fig. 6.1.1 and 6.1.2.

TRUTH TABLE 2 INPUT NOR

A	B	A+B
-.005	-.005	-5.0
-.005	-3.0	-.008
-3.0	-.005	-.008
-3.0	-3.0	-.008

TRUTH TABLE 4 INPUT NOR

A	B	C	D	$\overline{A+B+C+D}$
-0.005	-0.005	-0.005	-0.005	-5.0
-0.005	-0.005	-0.005	-3.0	-0.008
-0.005	-0.005	-3.0	-0.005	-0.008
-0.005	-0.005	-3.0	-3.0	-0.004
-0.005	-3.0	-0.005	-0.005	-0.008
-0.005	-3.0	-0.005	-3.0	-0.004
-0.005	-3.0	-3.0	-0.005	-0.004
-0.005	-3.0	-3.0	-3.0	-0.006
-3.0	-0.005	-0.005	-0.005	-0.008
-3.0	-0.005	-0.005	-3.0	-0.004
-3.0	-0.005	-3.0	-3.0	-0.006
-3.0	-3.0	-0.005	-0.005	-0.004
-3.0	-3.0	-0.005	-3.0	-0.006
-3.0	-3.0	-3.0	-0.005	-0.006
-3.0	-3.0	-3.0	-3.0	-0.002

The '0' and '1' inputs were applied by saturating and cutting off a transistor and applying it through a 1 way to 4 way adapter box.

Set 2 - Drive capability

Drive capabilities of TRL gates were tested by subjecting the gates to various forms of loading conditions and measuring the output. The circuit for this is shown in Fig. 7.1.3 and the tests were carried out at 25° C and 75° C.

DRIVE CAPABILITIES OF TRL GATES AT 25° C

Vin	$Vout_0$	$Vout_1$	Fan-out	Nature of Fan-out
-3V, 2 μs	-0.1V	-6.0V	0	
-3V, 2 "	-0.1V	-5.5V	1	
-3V, 2 "	-0.1V	-4.6V	2	TRL Gates
-3V, 2 "	-0.1V	-4.0V	3	
-3V, 2 "	-0.1V	-3.6V	4	
-3V, 2 "	-0.1V	-4.8V	1	
-3V, 2 "	-0.1V	-4.2V	2	
-3V, 2 "	-0.1V	-3.7V	3	Flip Flop
-3V, 2 "	-0.1V	-3.3V	4	
-3V, 2 "	-0.1V	-5.0V	1	
-3V, 2 "	-0.1V	-4.2V	2	
-3V, 2 "	-0.1V	-3.8V	3	Inverters
-3V, 2 "	-0.1V	-3.6V	4	
-3V, 2 "	-0.1V	-5.5V	1	
-3V, 2 "	-0.1V	-5.3V	2	
-3V, 2 "	-0.1V	-5.1V	3	One-shots
-3V, 2 "	-0.1V	-4.9V	4	

DRIVE CAPABILITY AT 75° C

Vin	$Vout_0$	$Vout_1$	Fan-out	Nature of Fan-out
-3V, 2 μs	-0.1V	-6.0V	0	
-3V, 2 "	-0.1V	-5.0V	1	
-3V, 2 "	-0.1V	-4.4V	2	TRL Gates
-3V, 2 "	-0.1V	-3.9V	3	
-3V, 2 "	-0.1V	-3.6V	4	
-3V, 2 "	-0.1V	-5.0V	1	
-3V, 2 "	-0.1V	-4.5V	2	Flip Flops
-3V, 2 "	-0.1V	-4.0V	3	
-3V, 2 "	-0.1V	-3.5V	4	
-3V, 2 "	-0.1V	-5.0V	1	
-3V, 2 "	-0.1V	-4.2V	2	Inverters
-3V, 2 "	-0.1V	-3.9V	3	
-3V, 2 "	-0.1V	-3.5V	4	
-3V, 2 "	-0.1V	-5.5V	1	
-3V, 2 "	-0.1V	-5.0V	2	One-shots
-3V, 2 "	-0.1V	-4.8V	3	
-3V, 2 "	-0.1V	-4.4V	4	

Set 3 - Transient Characteristics:

The gates are connected in a ring as shown in Fig. 7.1.4 and the input pulse is removed. The loop gain being greater than 1, the ring will oscillate and produce a square wave. The time period of the square wave is the sum of the delay of all stages and the delay per stage is given by the time period divided by the number of stages.

Period of soscillation = 3.05 μs

No. of stages = 7

Delay per stage = 3.05/7 = 450 nS

The rise, storage and fall times are measured using the circuit given in Fig. 7.1.5 and the stage delay measured by this method were compared to the previous value. These measurements give the delay according to the actual set of conditions existing in our circuit. The manufacturers specify a turn ON time of 65 nS and a turn OFF time of 125 nS giving a stage delay of 190 nS at I_c = 10 mA and I_b = 1 mA. The present measurements are at I_c = 6.7 mA and I_b = 0.34 mA which depict actual operating conditions and are listed below:

t_r (rise time)	120 nS
t_s (storage time)	180 nS
t_f (fall time)	140 nS
stage delay	440 nS

This compares well with our measured block delay.

Maximum operating frequency = $1/450 \times 10^{-9}$ = 2.2 Mc/s.

7.2 INVERTERS

Two sets of observations were recorded to find the performance of the inverter.

Set 1 - Drive Capability:

This set indicates the performance of inverter under extreme temperature conditions with loads of varying fan-outs. The circuit diagram for testing is given in Fig. 7.2.1 and measurements recorded below:

DRIVE CAPABILITY AT 25° C

Vin	$Vout_0$	$Vout_1$	Fan-out	Type of Fan-out
-3V, 2 μs	-0.1V	-6.0V	0	
-3V, 2 "	-0.1V	-5.0V	1	
-3V, 2 "	-0.1V	-4.5V	2	TRL Gates
-3V, 2 "	-0.1V	-4.2V	3	
-3V, 2 "	-0.1V	-3.75V	4	
-3V, 2 "	-0.1V	-5.25V	1	
-3V, 2 "	-0.1V	-4.75V	2	Inverters
-3V, 2 "	-0.1V	-4.25V	3	
-3V, 2 "	-0.1V	-3.5V	4	
-3V, 2 "	-0.1V	-5.2V	1	
-3V, 2 "	-0.1V	-4.8V	2	Flip Flops
-3V, 2 "	-0.1V	-4.0V	3	
-3V, 2 "	-0.1V	-3.8V	4	
-3V, 2 "	-0.1V	-5.8V	1	
-3V, 2 "	-0.1V	-5.4V	2	One-shots
-3V, 2 "	-0.1V	-5.0V	3	
-3V, 2 "	-0.1V	-4.6V	4	

DRIVE CAPABILITY AT 75° C

Vin	V_{out_0}	V_{out_1}	Fan-out	Type of Fan-out
-3V, 2 μs	-0.1V	-6.0V	0	
-3V, 2 "	-0.1V	-5.4V	1	
-3V, 2 "	-0.1V	-4.6V	2	Inverters
-3V, 2 "	-0.1V	-4.0V	3	
-3V, 2 "	-0.1V	-3.6V	4	
-3V, 2 "	-0.1V	-5.4V	1	
-3V, 2 "	-0.1V	-4.6V	2	
-3V, 2 "	-0.1V	-4.1V	3	TRL Gates
-3V, 2 "	-0.1V	-3.8V	4	
-3V, 2 "	-0.1V	-5.4V	1	
-3V, 2 "	-0.1V	-4.8V	2	
-3V, 2 "	-0.1V	-4.1V	3	Flip Flop
-3V, 2 "	-0.1V	-3.8V	4	
-3V, 2 "	-0.1V	-5.8V	1	
-3V, 2 "	-0.1V	-5.4V	2	
-3V, 2 "	-0.1V	-5.0V	3	One-shots
-3V, 2 "	-0.1V	-4.6V	4	

Set 2 - Measurement of Transient Characteristics:

The transient characteristics are specified by the rise, storage and fall times. These are measured by applying a -3V , 0.1 μs, input pulse and comparing it with the output. The circuit for the experiment is shown in Fig. 7.2.2 and results are as follows:

t_r = rise time = 15 nS

t_s = storage time = 5 nS

t_f = fall time = 15 nS

delay per stage 35 nS

Stage Delay by Ring Oscillator Method:

As in the case of TRL gates, 7 inverters are connected in cascade in the form of a ring oscillator as shown in Fig. 7.2.2 and period of oscillation measured.

Period of oscillation = 250 nS

Number of stages = 7

Delay per stage = 250/7 = 35 nS.

This compares favourably with the previous results.

7.3 FLIP FLOP

Three sets of tests are carried out on flip flops to find its performance.

Set 1 - Input Characteristics:

On receiving an input pulse at the D.C. set & reset and pulse set & reset terminals, the flip flop must change state if it was in the complementary state. There must be no change of state if the previous state was a state for which the input was received. An input at the trigger terminal will change state of flip flop immaterial to its previous state.

These tests have been carried out at 25° C, 75° C and 0° C, and are found to operate satisfactorily. Records for 0° C have not been given.

The input characteristics are verified by the block diagram shown in Fig. 7.3.1 and results are tabulated below:

INPUT CHARACTERISTICS AT 25° C

Ampli-tude	Pulse width	Input terminal	Output	Complementary output	Load
-3V	-	D.C. set	-4.8V	-0.1V	
-3V	-	D.C. reset	-0.1V	-5.2V	
-3V	2.0 us	Pulse set	-4.8V	-0.1V	No load
-3V	2.0 us	Pulse reset	-6.1V	-5.2V	
-3V	0.1 us,500Kc/s	Trigger	-4.8V,2 us @ 250 Kc/s	-5.2V,2 us @ 250 Kc/s	
-3V	-	D.C. set	-4.0V	-0.1V	Unbalanced
-3V	-	D.C. reset	-0.1V	-5.4V	Load of
-3V	2.0 us	Pulse set	-4.0V	-0.1V	1.5K on Y
-3V	2.0 us	Pulse reset	-0.1V	-5.4V	
-3V	0.1 us,500Kc/s	Trigger	-4.0V,2 us @ 250 Kc/s	-5.4V,2 us @ 250 Kc/s	
-3V	-	D.C. set	-4.8V	-0.1V	Unbalanced
-3V	-	D.C. reset	-0.1V	-4.2V	Load of
-3V	2.0 us	Pulse set	-4.8V	-0.1V	1.5K on $\bar{Y}$
-3V	2.0 us	Pulse reset	-0.1V	-4.2V	
-3V	0.1 us,500Kc/s	Trigger	-4.8V,2 us @ 250 Kc/s	-4.2V,2 us @ 250Kc/s	
-3V	-	D.C. set	-3.4V	-0.1V	Balanced
-3V	-	D.C. reset	-0.1V	-3.6V	Load of
-3V	2.0 us	Pulse set	-3.4V	-0.1V	1.5K
-3V	2.0 us	Pulse reset	-0.1V	-3.6V	
-3V	0.1 us,500Kc/s	Trigger	-3.4V,2 us @ 250 Kc/s	-3.6V,2 us @ 250 Kc/s	

INPUT CHARACTERISTICS AT 75° C

Amplitude	Pulse width	Input terminal	Output	Complementary output	Load
-4V	-	D.C. set	-4.9V	-0.1V	
-4V	-	D.C. reset	-0.1V	-5.1V	
-4V	2.0 us	Pulse set	-4.9V	-0.1V	No load
-4V	2.0 us	Pulse reset	-0.1V	-5.1V	
-3V	0.1 us, 500Kc/s	Trigger	-4.9V,2 us @ 250Kc/s	-5.1V,2 us @ 250 Kc/s	
-4V	-	D.C. set	-3.5V	-0.1V	Balanced
-4V	-	D.C. reset	-0.1V	-3.5V	Load of
-4V	2.0 us	Pulse set	-3.5V	-0.1V	1.5 K
-4V	2.0 us	Pulse reset	-0.1V	-3.5V,	
-3V	0.1 us 500Kc/s	Trigger	-3.5V,2us @ 250Kc/s	-3.5V,2us @ 250Kc/s	
-4V	-	D.C. set	-3.5V	-0.1V	
-4V	-	D.C. reset	-0.1V	-5.0V	Unbalanced
-4V	2.0 us	Pulse set	-3.5V	-0.1V	Load of
-4V	2.0 us	Pulse reset	-0.1V	-5.0V	1.5 K on Y
-3V	0.1 us 500 Kc/s	Trigger	-3.5V,2us @ 250Kc/s	-5.0V,2us @ 250Kc/s	
-4V	-	D.C. set	-4.8V	-0.1V	
-4V	-	D.C. reset	-0.1V	-3.5V	Unbalanced
-4V	2.0 us	Pulse set	-4.8V	-0.1V	Load of
-4V	2.0 us	Pulse reset	-0.1V	-3.5V	1.5 K on $\bar{Y}$
-3V	0.1 us 500 Kc/s	Trigger	-4.8V,2us @ 250Kc/s	-3.5V,2us @ 250Kc/s	

Trigger sensitivity:

Flip flop is triggered by negative going edge of input pulse.

Minimum trigger amplitude -2.0V

Erratic triggering between -2.0V and -2.5V

Stable triggering above -2.5V

Maximum acceptable trigger amplitude -8V

Set 2 - Drive Capability:

This indicates the driving capability of flip flop under loading conditions. The flip flop is driven at 500 Kc/s with an input pulse of 2 us as shown in Fig. 7.3.2. A load of 1.5K is applied at $\bar{Y}$ output at pin 4 and loads of varying fan-out applied at Y output. The measurements of Y output are recorded at 25° C and 70° C

DRIVE CAPABILITY AT 25° C

Vin at trigger	$Vout_0$	$Vout_1$	Fan-out	Nature of Fan-out
-3V, 2 us	-0.1V	-5.2V	0	
-3V, 2 us	-0.1V	-4.4V	1	
-3V, 2 us	-0.1V	-4.0V	2	Flip Flops
-3V, 2 us	-0.1V	-3.7V	3	
-3V, 2 us	-0.1V	-3.4V	4	
-3V, 2 us	-0.1V	-4.6V	1	
-3V, 2 us	-0.1V	-4.0V	2	Inverters
-3V, 2 us	-0.1V	-3.6V	3	
-3V, 2 us	-0.1V	-3.4V	4	
-3V, 2 us	-0.1V	-4.8V	1	
-3V, 2 us	-0.1V	-4.6V	2	One-shots
-3V, 2 us	-0.1V	-4.4V	3	
-3V, 2 us	-0.1V	-4.2V	4	
-3V, 2 us	-0.1V	-4.2V	1	
-3V, 2 us	-0.1V	-3.9V	2	TRL Gates
-3V, 2 us	-0.1V	-3.6V	3	
-3V, 2 us	-0.1V	-3.4V	4	

DRIVE CAPABILITY AT 75° C

Vin at trigger	$Vout_0$	$Vout_1$	Fan-out Y	Nature of Fan-out
-3V, 2 us	-0.1V	-5.4V	0	
-3V, 2 us	-0.1V	-4.6V	1	
-3V, 2 us	-0.1V	-4.0V	2	Flip Flops
-3V, 2 us	-0.1V	-3.7V	3	
-3V, 2 us	-0.1V	-3.4V	4	
-3V, 2 us	-0.1V	-4.8V	1	
-3V, 2 us	-0.1V	-4.0V	2	Inverters
-3V, 2 us	-0.1V	-3.9V	3	
-3V, 2 us	-0.1V	-3.6V	4	
-3V, 2 us	-0.1V	-5.1V	1	
-3V, 2 us	-0.1V	-4.8V	2	One-shots
-3V, 2 us	-0.1V	-4.6V	3	
-3V, 2 us	-0.1V	-4.2V	4	
-3V, 2 us	-0.1V	-4.4V	1	
-3V, 2 us	-0.1V	-4.0V	2	TRL Gates
-3V, 2 us	-0.1V	-3.8V	3	
-3V, 2 us	-0.1V	-3.4V	4	

Set 3 - Transient Characteristics:

This set indicates the results of transient tests where rise time, fall time and storage time are measured. The measurements were done by triggering the flip flop and the transient times (i.e., t_r, t_s and t_f) were measured on the oscilloscope.

t_r	(rise time)	35 ns
t_s	(storage time)	60 ns
t_f	(fall time)	250 ns
	stage delay	345 ns

Maximum operating frequency = $1/345 \times 10^{-5}$ = 1.55 Mc/s.

The flip flops were driven at 1.25 Mc/s by a programmable pulse generator and they were found to operate satisfactorily.

7.4 MONOSTABLE MULTIVIBRATOR

Set 1 -

This indicates variation of pulse width for varying C_D. The pulse width can be calculated from equation 5.2.8 and is given by

$$T_D = C_D R_D \ln((V^*_{ce}+I^*_{bl_2}R_D+V^*_s-V^*_{ces1}-V^*_{bes2})/(V^*_{cc}-V_{tf_2}+I^*_{bl_2}R_D))$$

$$= .51\, C_D R_D$$

The variation of T_D with C_D for R_D nominal of 15 K is given below and the experimental set up is shown in Fig. 7.4.1. The measurements were made at 25° C.

VARIATION OF T_D WITH C_D

S.No.	C_D	T_D	S.No.	C_D	T_D
1	10 pf	0.02 μs	15	180 pf	1.08 μs
2	12 pf	0.03 μs	16	220 pf	1.22 μs
3	18 pf	0.075 μs	17	270 pf	1.46 μs
4	22 pf	0.1 μs	18	370 pf	1.94 μs
5	27 pf	0.14 μs	19	390 pf	2.25 μs
6	33 pf	0.18 μs	20	470 pf	2.5 μs
7	39 pf	0.2 μs	21	680 pf	4.0 μs
8	47 pf	0.28 μs	22	820 pf	4.8 μs
9	56 pf	0.36 μs	23	2200 pf	13.0 μs
10	68 pf	0.42 μs	24	3300 pf	19.0 μs
11	82 pf	0.50 μs	25	4700 pf	23.5 μs
12	100 pf	0.58 μs	26	.047 uf	270 μs
13	120 pf	0.68 μs	27	.01 uf	62.5 μs
13	150 pf	0.88 μs	28	4.0 uf	28.0 ms

Set 2 - Drive Capability:

The drive capability of one-shots is found with the circuit shown in Fig. 7.4.1. The one-shot is driven by a 0.1 us, 500 Kc/s input at pin 4. For the values of capacitance chosen, the output pulse width is 2 us. The terms in the table are defined below:

V_{o0} - output for a '0' level

V_{o1} - output for a '1' level

V_{c0} - complementary output for a '0' level

V_{c1} - complementary output for a '1' level

Tr - input trigger amplitude.

DRIVE CAPABILITY AT 25° C

Tr	V_{o0}	V_{o1}	V_{c0}	V_{c1}	Fan-out	in
-3V	-0.1V	-4.5V	-0.1V	-3.25V	1	Inverters
-3V	-0.1V	-4.0V	-0.1V	-3.25V	2	
-3V	-0.1V	-3.5V	-0.1V	-3.25V	3	
-3V	-0.1V	-3.25V	-0.1V	-3.25V	4	
-3V	-0.1V	-4.6V	-0.1V	-3.25V	1	Flip flops
-3V	-0.1V	-4.0V	-0.1V	-3.25V	2	
-3V	-0.1V	-3.5V	-0.1V	-3.25V	3	
-3V	-0.1V	-3.2V	-0.1V	-3.25V	4	
-3V	-0.1V	-6.0V	-0.1V	-3.25V	0	TRL Gates
-3V	-0.1V	-4.4V	-0.1V	-3.25V	1	
-3V	-0.1V	-4.0V	-0.1V	-3.25V	2	
-3V	-0.1V	-3.6V	-0.1V	-3.25V	3	
-3V	-0.1V	-3.3V	-0.1V	-3.25V	4	
-3V	-0.1V	-3.1V	-0.1V	-3.25V	5	
-3V	-0.1V	-5.0V	-0.1V	-3.25V	1	One-shots
-3V	-0.1V	-4.8V	-0.1V	-3.25V	2	
-3V	-0.1V	-4.5V	-0.1V	-3.25V	3	
-3V	-0.1V	-4.3V	-0.1V	-3.25V	4	

DRIVE CAPABILITY AT 75° C

Tr	V_{o0}	V_{o1}	V_{c0}	V_{c1}	Fan-out	Nature of Fan-out
-3V	-0.1V	-6.0V	-0.1V	-3.5V	0	
-3V	-0.1V	-5.4V	-0.1V	-3.5V	1	
-3V	-0.1V	-4.8V	-0.1V	-3.5V	2	Inverters
-3V	-0.1V	-4.4V	-0.1V	-3.5V	3	
-3V	-0.1V	-4.0V	-0.1V	-3.5V	4	
-3V	-0.1V	-5.2V	-0.1V	-3.5V	1	
-3V	-0.1V	-4.8V	-0.1V	-3.5V	2	Flip Flops
-3V	-0.1V	-4.4V	-0.1V	-3.5V	3	
-3V	-0.1V	-4.0V	-0.1V	-3.5V	4	
-3V	-0.1V	-5.6V	-0.1V	-3.5V	1	
-3V	-0.1V	-5.3V	-0.1V	-3.5V	2	One-shots
-3V	-0.1V	-5.0V	-0.1V	-3.5V	3	
-3V	-0.1V	-4.6V	-0.1V	-3.5V	4	
-3V	-0.1V	-5.4V	-0.1V	-3.5V	1	
-3V	-0.1V	-4.8V	-0.1V	-3.5V	2	TRL Gates
-3V	-0.1V	-4.4V	-0.1V	-3.5V	3	
-3V	-0.1V	-4.0V	-0.1V	-3.5V	4	

Set 3 - Measurement of Transient Characteristics:

t_r (rise time) 40 ns

t_f (fall time) 100 ns

stage delay 140 ns

Trigger Sensitivity:

Minimum trigger amplitude to trigger monostable = ..75V.

7.5 LAMP DRIVERS

Three sets of tests are performed on lamp drivers.

Set 1 - D.C. Conditions:

The circuit diagram for the test is shown in Fig. 7.5.1 and the results are tabulated below:

Vin	I_{b_1}	I_{b_2}	I_{c_2}	State of lamp
-0.3V	-	-	-	Lamp OFF
-3.0V	22uA	5mA	132mA	Lamp ON

Minimum I_{c_2} for lamp to light = 70 mA

Minimum I_{b_2} for lamp to light = 3.5 mA

Maximum I_{b_2} for which lamp will not light = 3.2 mA

Minimum I_{c_1} for lamp to light = 3.5 mA

Minimum V_{b_1} for lamp to light = -1.2 V

Minimum I_{b_1} for lamp to light

Set 2 - Temperature Test:

The lamp card was left in the oven at 75° C and -3V applied at the input. This did not turn ON the lamp. This ensures I_{cbo} of Q_1 cannot turn ON the lamp at high temperature.

Set 3 - Pulse Test:

A -3V, 16 c/s input is applied at the lamp driver input. The lamp turns ON or OFF at 16 c/s.

7.6 TESTS ON NOISE IMMUNITY

Fig. 7.6.1 shows a circuit to test a card subjected to noise of -2V obtained by switching ON and OFF a relay operated switch across 720 Ω resistance. The arrangement changes a supply to the collector of each card from -6V to -8V and back at 100 c/s. This is equivalent to a -6V supply superimposed by a -2V noise. All circuits were found to operate satisfactorily under such conditions.

Immunity to radiated noise was tested by allowing a switch to spark in close vicinity of the card being tested. All circuits were found to operate satisfactorily under such conditions.

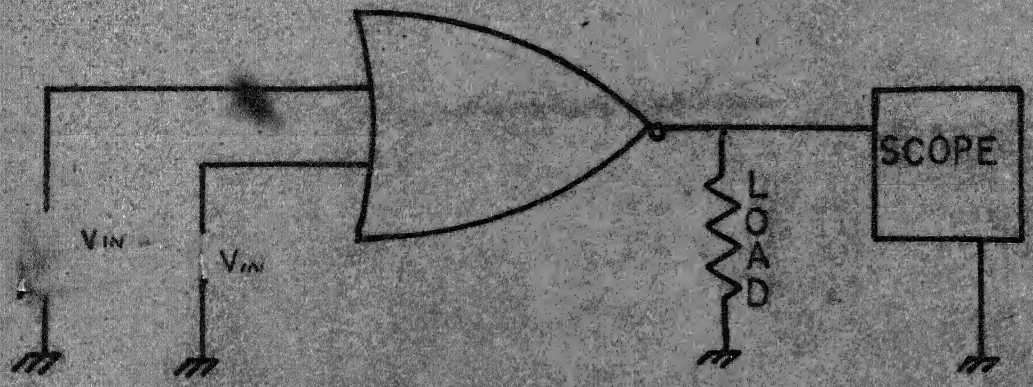


FIG.7.1.1:- CIRCUIT TO RECORD TRUTH TABLE FOR 2 INPUT NOR

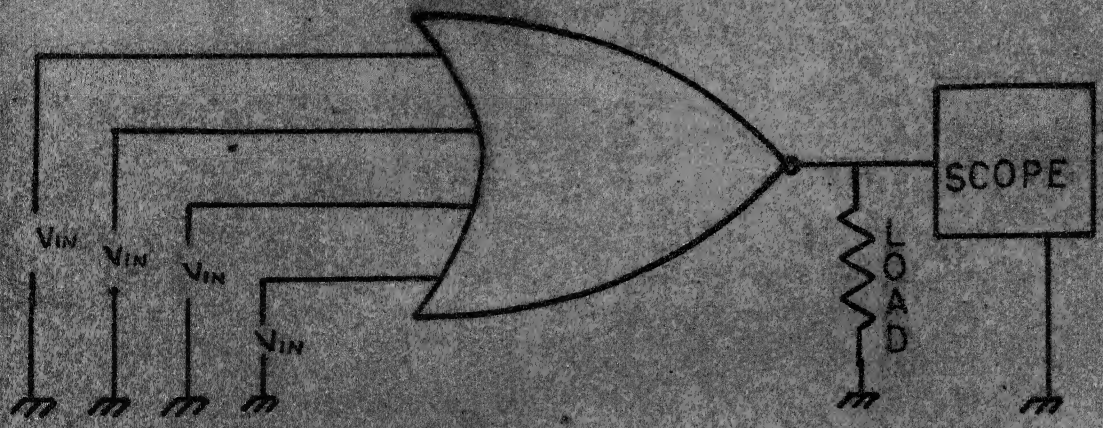


FIG.7.1.2:-CIRCUIT RECORD TRUTH TABLE FOR 4 INPUT NOR

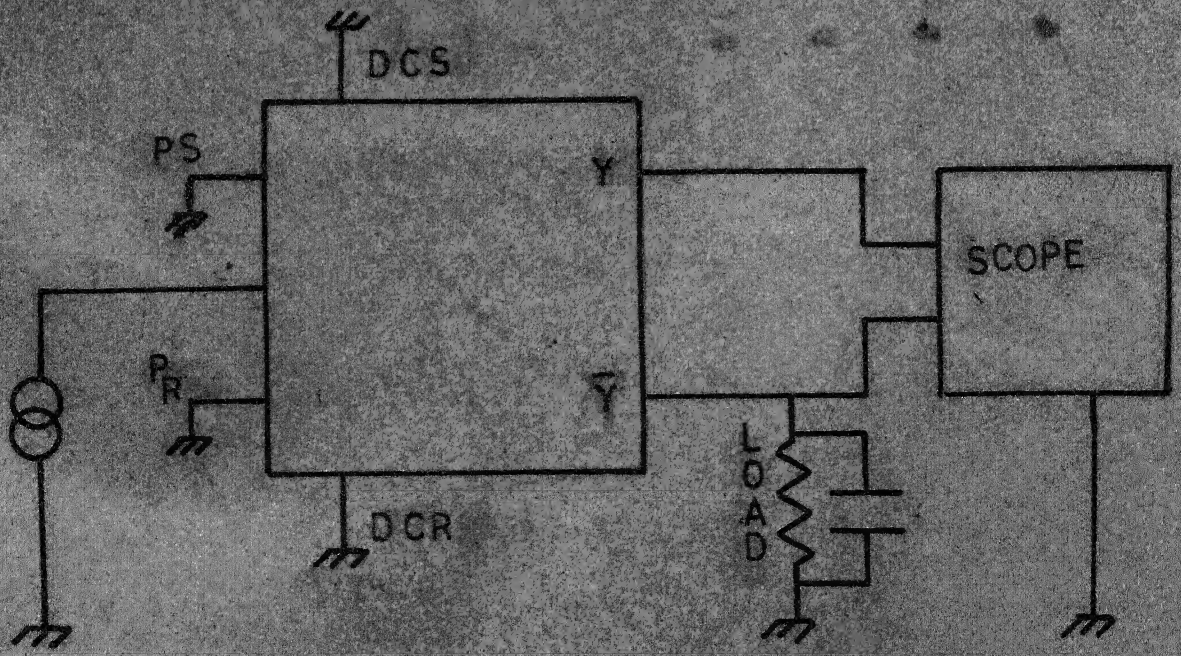


FIG.7.3.2:-CIRCUIT TO MEASURE DRIVE CAPABILITY OF FLIP FLOP

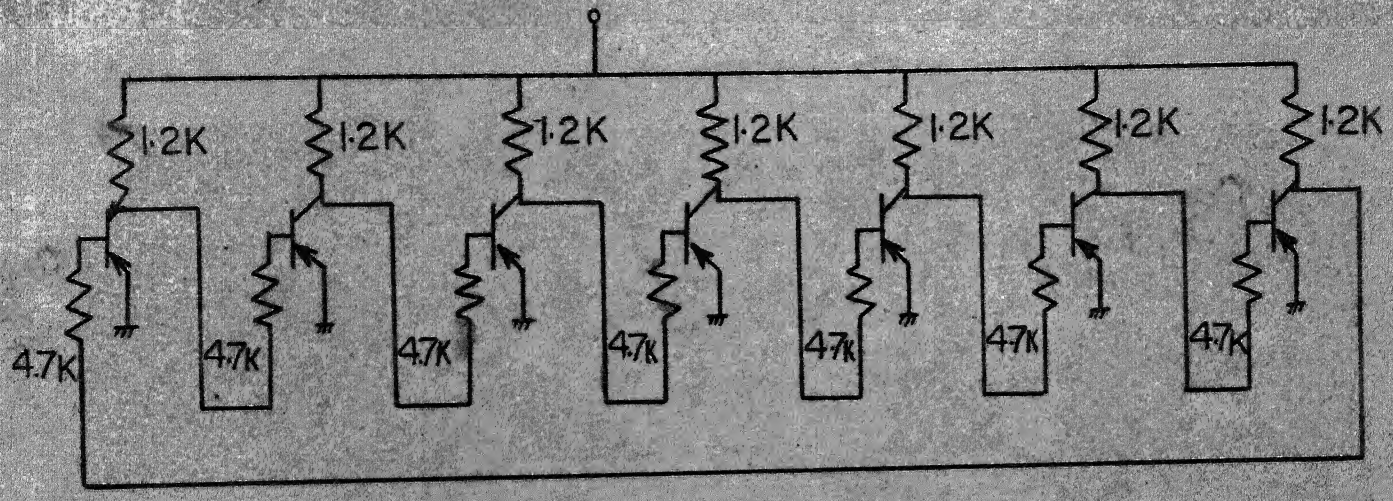


FIG.7·1·4 SEVEN NOR GATES CONNECTED As A RING OSCILLATOR

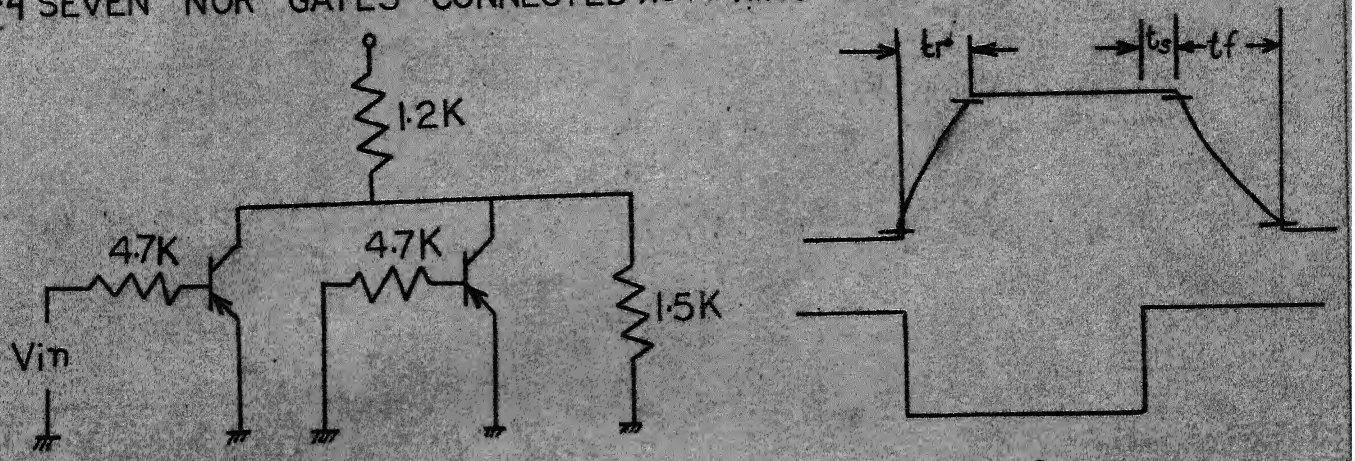


FIG 7·1·5 MEASUREMENT OF TRANSIENT CHARACTERISTICS

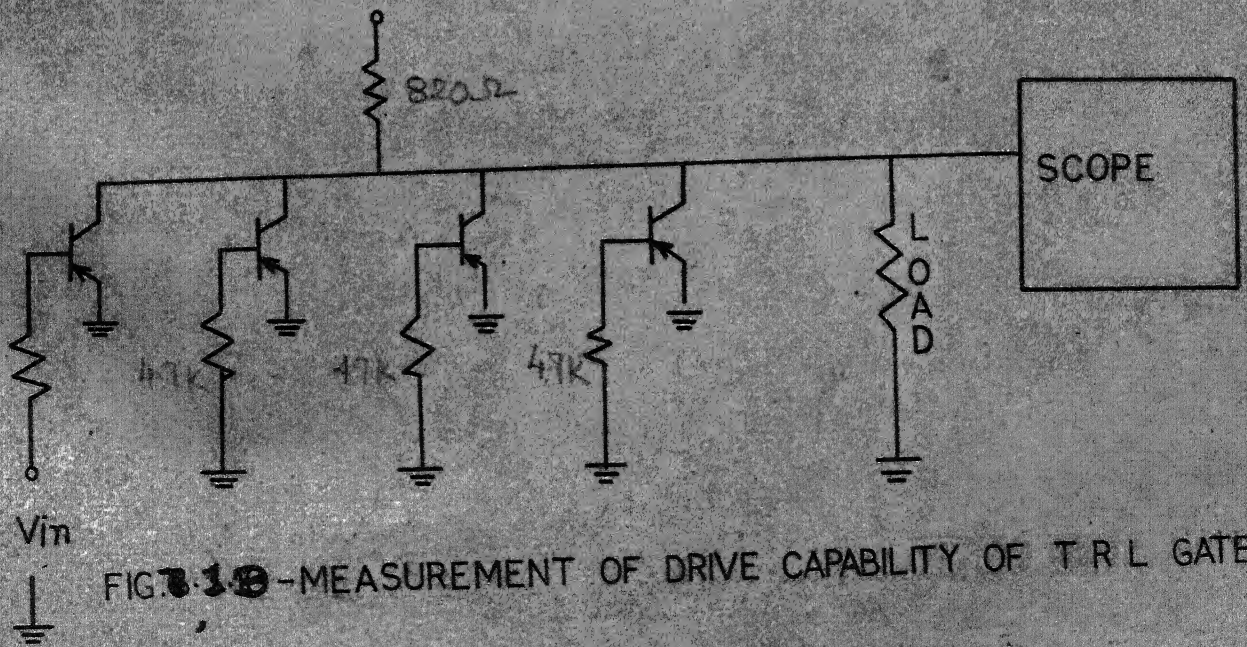


FIG.7·1·6 -MEASUREMENT OF DRIVE CAPABILITY OF T R L GATES

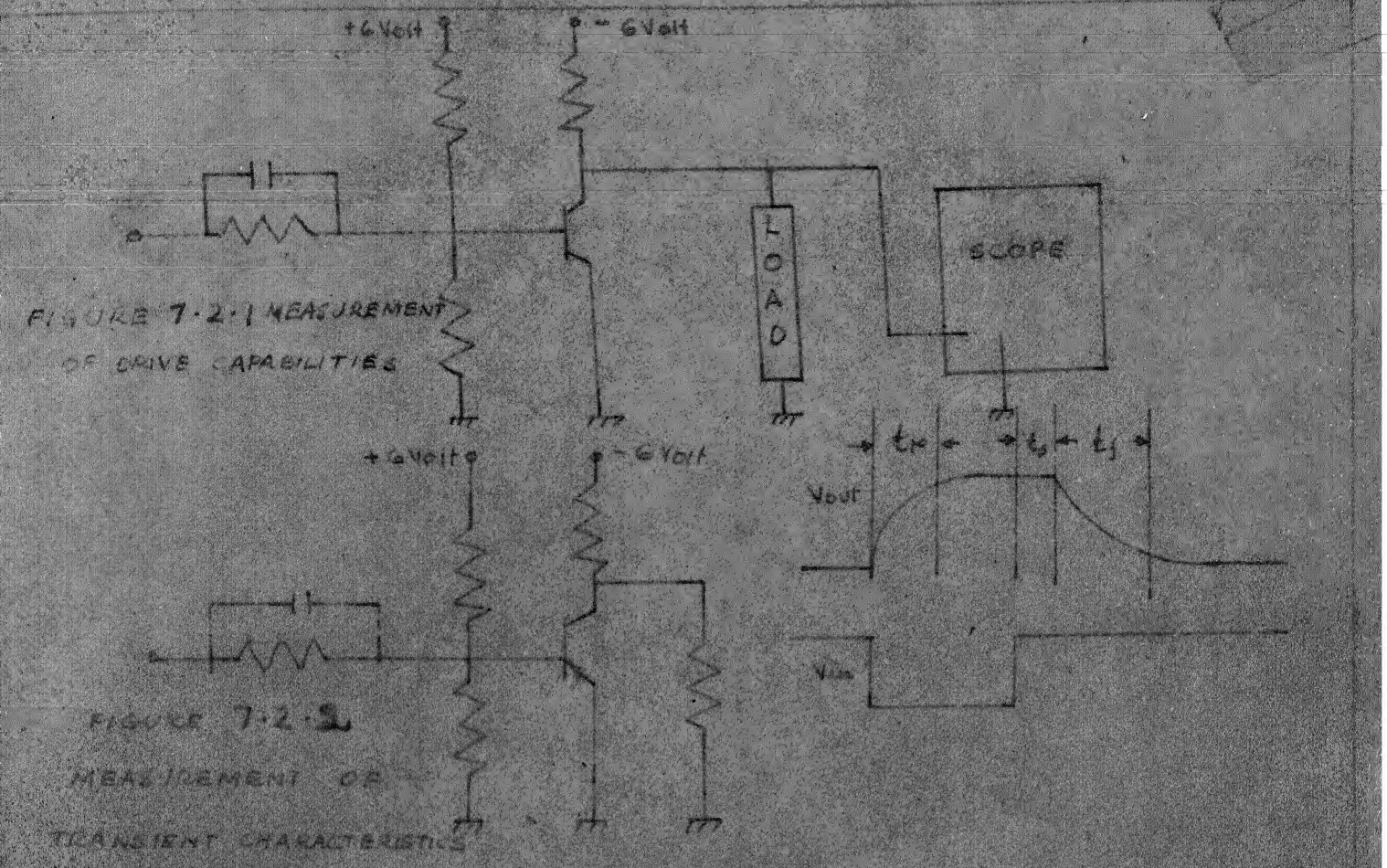


FIGURE 7.2.1 MEASUREMENT OF DRIVE CAPABILITIES

FIGURE 7.2.2 MEASUREMENT OF TRANSIENT CHARACTERISTICS

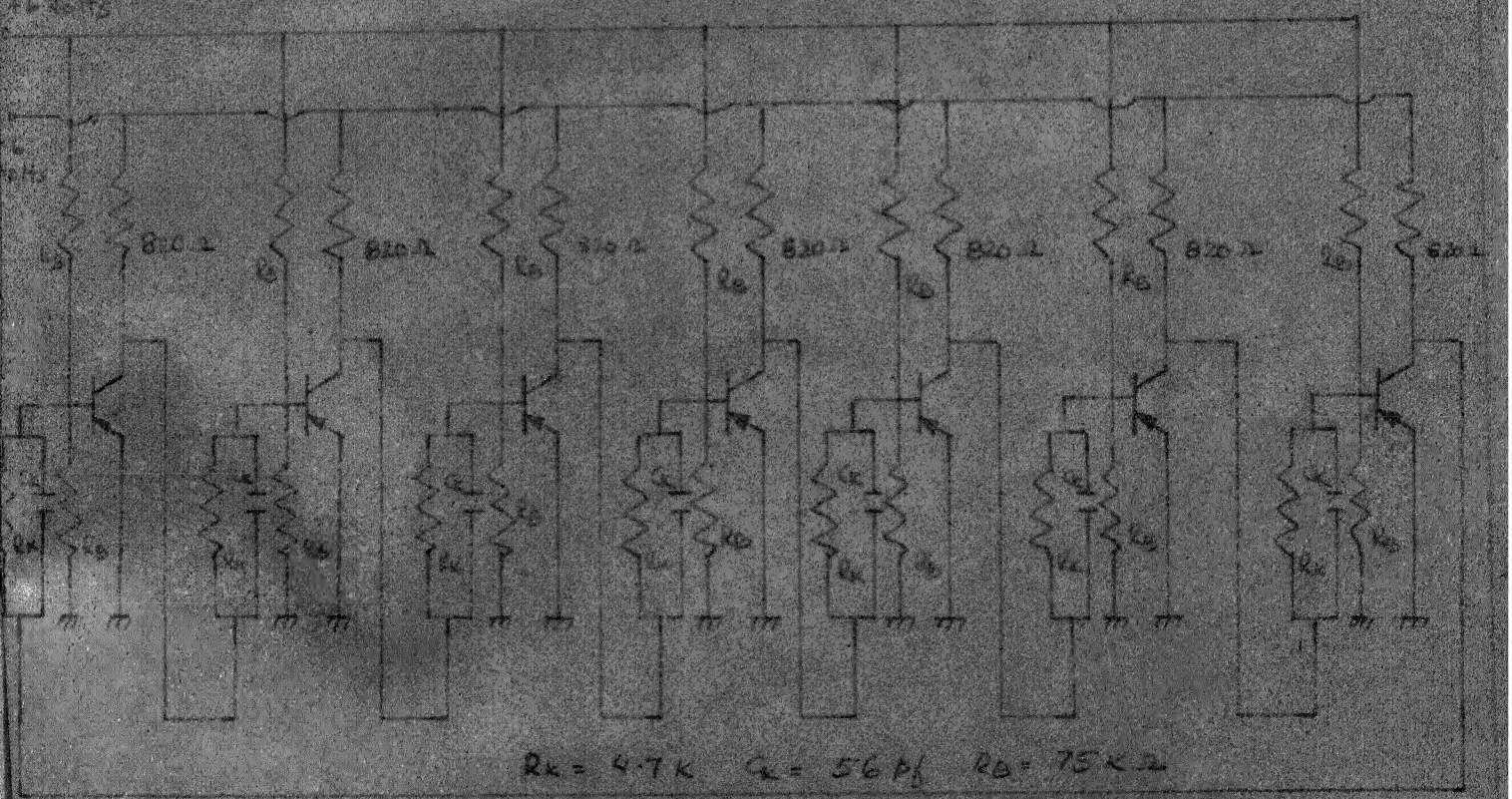


FIGURE 7.2.3 SEVEN INVERTERS CONNECTED AS RING OSCILLATOR

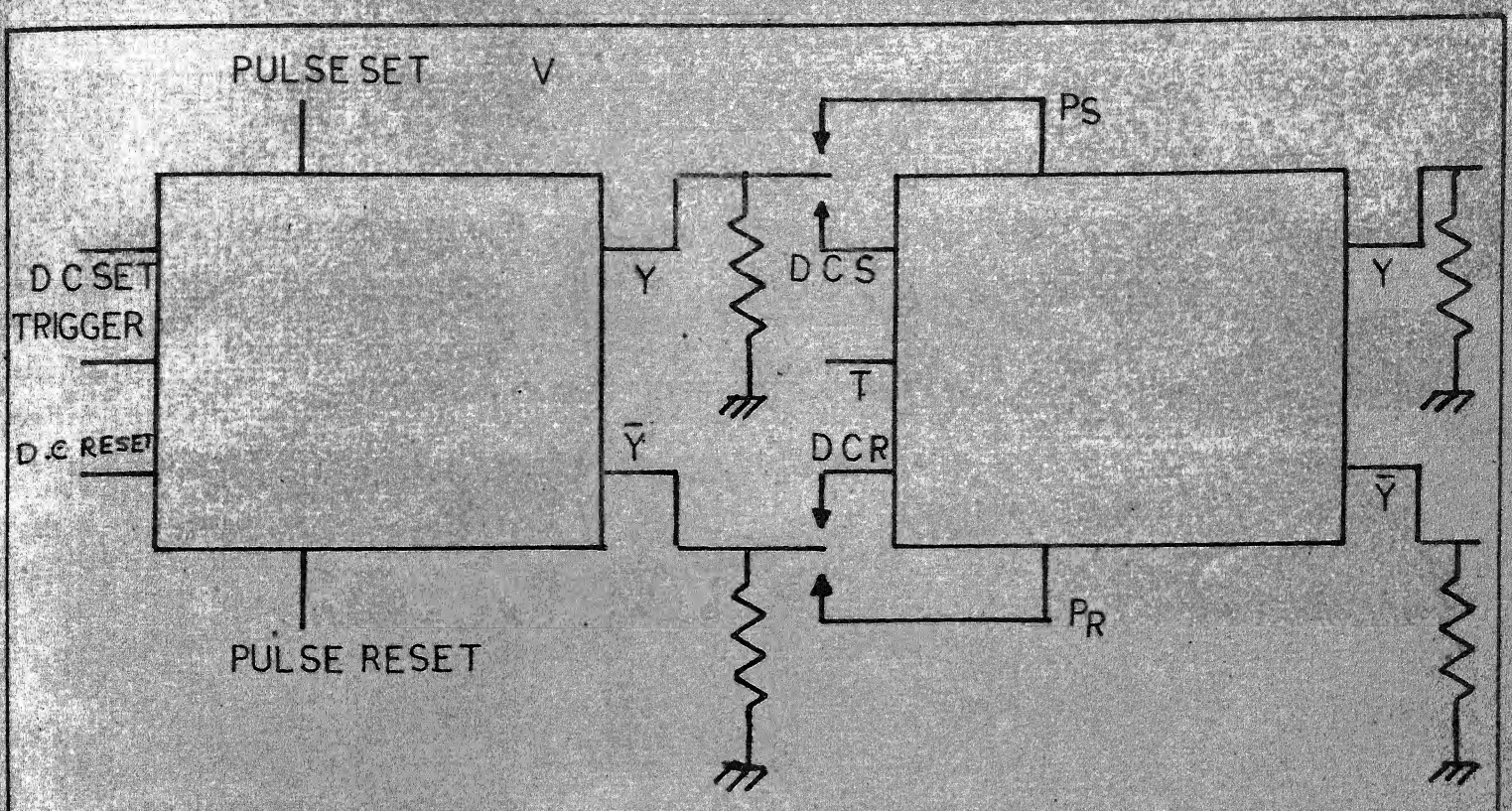
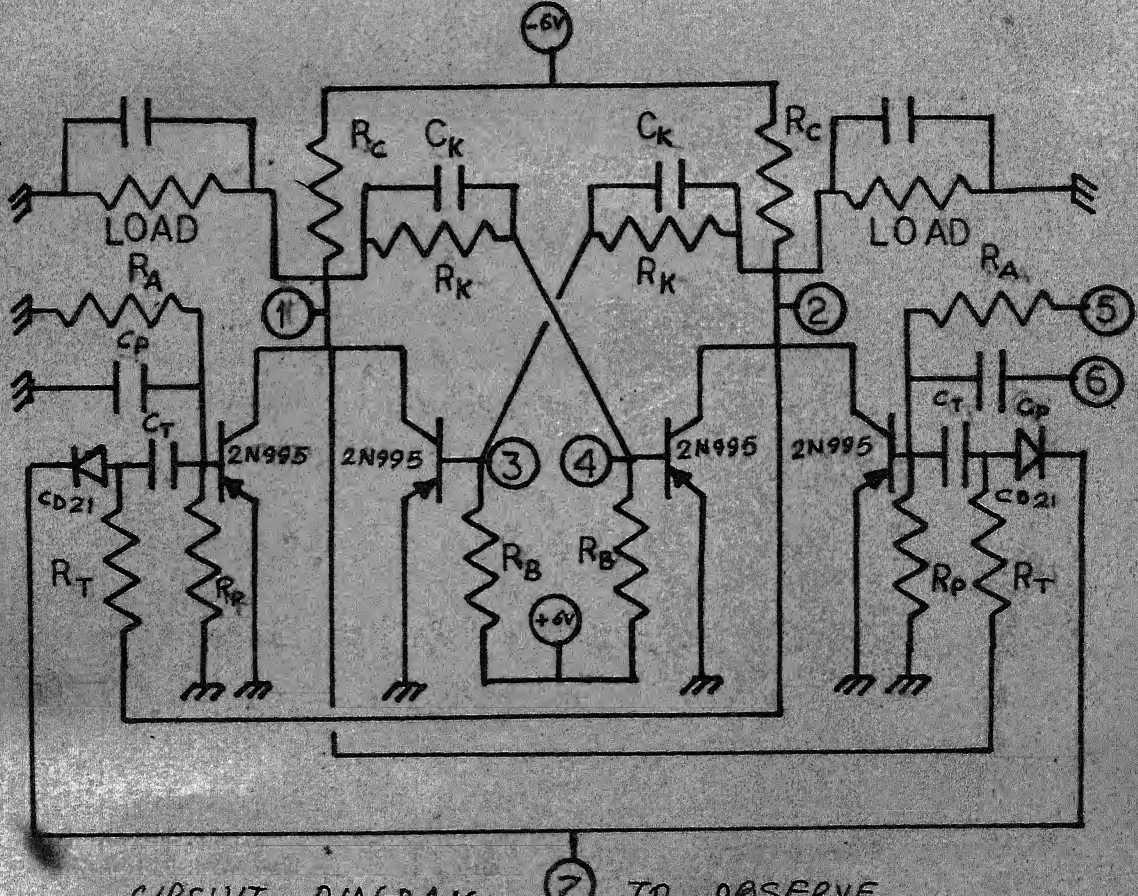


FIG.731 MEASUREMENT OF INPUT CHARACTERISTICS OF FLIP FLOP

C_K=56 pf
C_P=82 pf
C_T=56 pf
R_C=820 Ω
R_B=75K
R_A=4.7K
R = 4.7K
R_K=47K



CIRCUIT DIAGRAM TO OBSERVE

FIG.7.3.2:-WAVEFORMS OF FLIP FLOP TRIGGERED AT 500K C/S

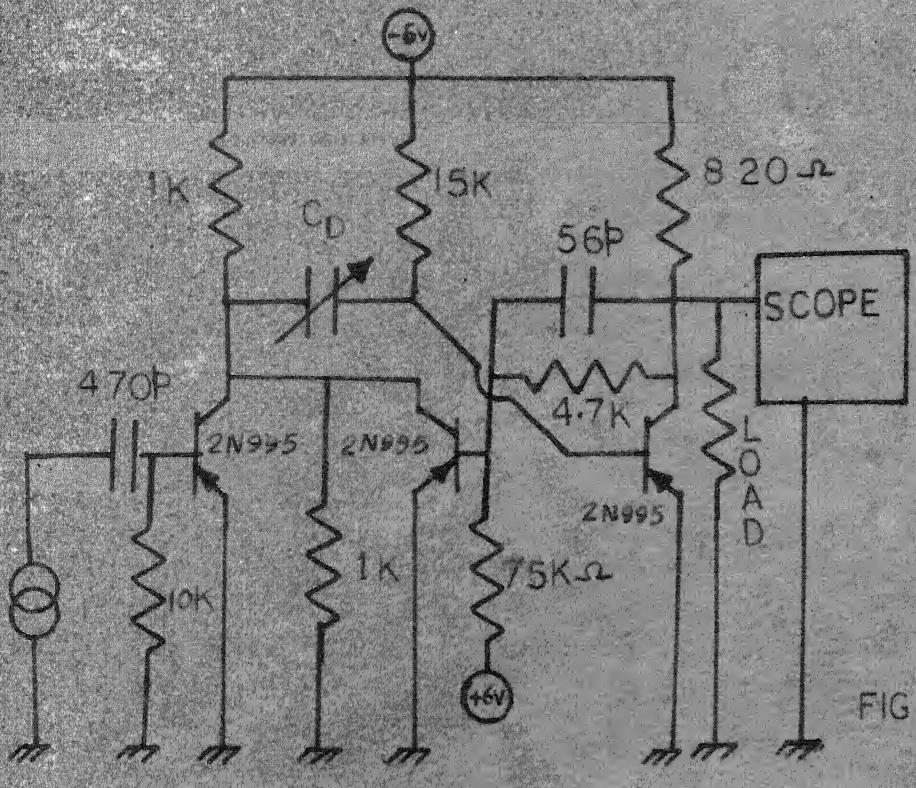


FIG.7.4.1:-TO MEASURE VARIATION OF T_D WITH C_D

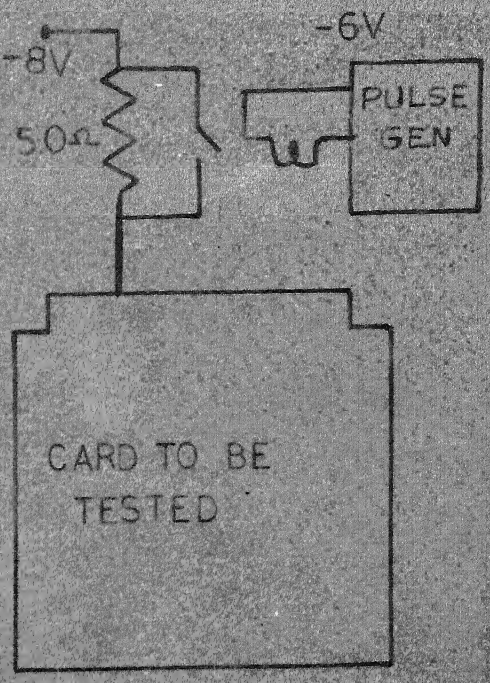


FIG 7.6.1 TEST ON NOISE IMMUNITY

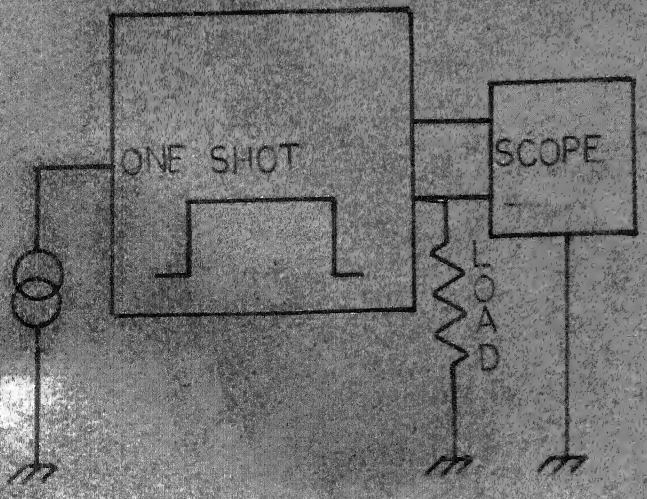


FIG.7.4.2 :-DRIVE CAPABILITY OF ONE SHOTS

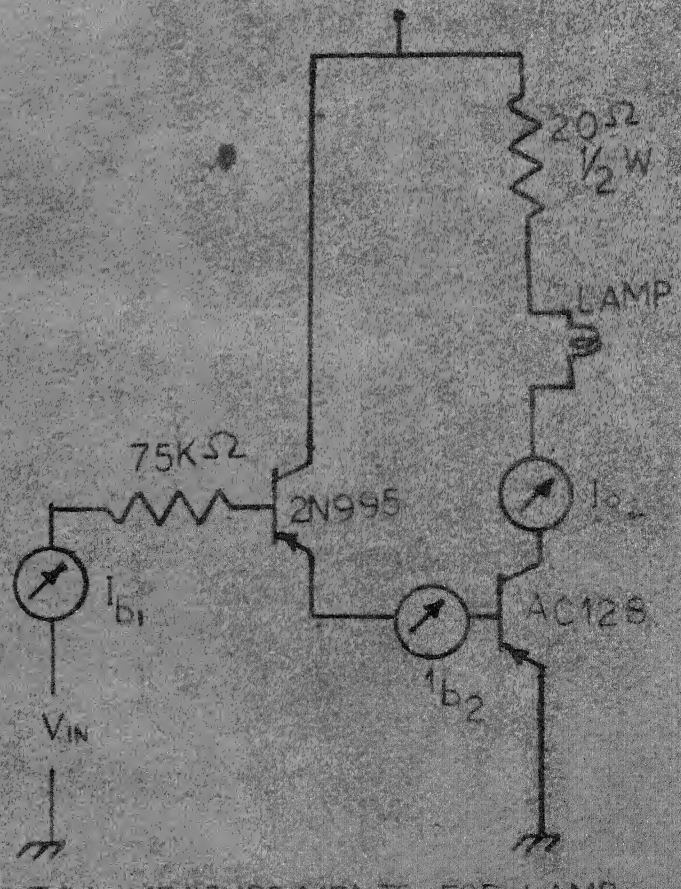


FIG.7.5.1:-MEASUREMENTS FOR LAMP DRIVERS

CHAPTER 8

CONCLUSION

Though prototype of all circuits were built during the project, mass production techniques have yet to be worked out in detail. The test procedures outlined are basically laboratory type tests and are not suitable for assembly line manufacture. Test jigs with GO and NO GO standards have to be designed with simple operating instructions to suit the Indian market availability situation of skilled and unskilled labour.

The standards of performance achieved by the basic modules lead one to conclude that it will be possible to build simple digital systems using entirely indigenous components.

APPENDIX - 1

INDIGENOUS SWITCHING TRANSISTOR PARAMETERS

Parameter	Type					
	2N404	2N428	2N995	CIL 701	CIL 711	CIL 511
V_{cbo} (Volts)	-25	-30	-20	32	60	20
V_{ebo} "	-12	-12	-4	7	7	5
V_{eco} "	-24	-20	-15	32	60	20
I_c (mA)	100	400	40	60	60	150
$I_{c_{max}}$ (mA)	1000	1000	60	200	200	150
V_{ces} @	-.1	-.35	-.2	.4	.4	.25
I_c (mA)	12	200	20	25	25	30
I_b (mA)	4	10	2	2.5	2.5	1.5
V_{bes} (Volts)@	-.25	-.6	-.7	.95	.95	.75
I_c (mA)	12	200	20	20	25	30
I_b (mA)	4	10	2	2	2.5	1.5
t_r	2us	40us	120ns	150ns	150ns	100ns
t_s	6us	30us	140ns	175ns	175ns	2us
t_f	20us	30us	180ns	75ns	75ns	140ns
$h_{FE_{min}}$	24	20	35	65	65	40

APPENDIX - 2

TRANSIENT TIMES OF INDIAN SWITCHING TRANSISTORS

CIL 701	1	2	3	4	5	6	7	8	9	10
t_r	.1	.07	.08	.07	.08	.07	.08	.07	.07	.08
t_s	2.5	4.0	2.2	3.0	4.0	3.0	2.5	3.0	2.8	2.5
t_f	0.9	0.75	1.0	0.8	0.5	0.8	0.75	0.8	0.8	0.75
Stage delay	3.5	4.82	3.28	3.87	4.58	3.87	3.33	3.87	3.67	3.33

CIL 711	1	2	3	4	5	6	7	8	9	10
t_r	.07	.08	.1	.07	.08	.09	.10	.07	.08	.09
t_s	2.5	3.2	4.2	3.0	3.5	3.0	4.0	2.5	2.8	3.5
t_f	1.0	0.8	0.5	0.6	0.75	0.8	0.8	0.75	1.0	0.9
Stage delay	3.57	4.08	4.8	3.67	4.33	3.89	4.9	3.32	3.88	4.49

CIL 511	1	2	3	4	5	6	7	8	9	10
t_r	.08	.1	.1	.08	.1	.1	.1	.1	.08	.09
t_s	2.0	1.6	2.0	2.0	3.0	1.5	1.8	3.0	2.5	2.0
t_f	0.8	0.8	1.0	0.8	0.9	1.0	1.0	0.8	0.75	0.8
Stage delay	2.88	2.5	3.1	2.88	4.0	2.6	2.9	3.9	3.33	2.89

2N995	1	2	3	4	5	6	7	8	9	10
t_r	.12	.11	.13	.10	.08	.11	.12	.08	.08	.11
t_s	.18	.18	.18	.14	.12	.18	.18	.12	.12	.18
t_f	.14	.14	.14	.14	.10	.14	.14	.10	.10	.14
Stage delay	.44	.43	.45	.38	.30	.43	.44	.30	.30	.43

All times are in micro-seconds.

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